Networks · Communications

DELUA User's Guide

EK-DELUA-UG-002

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DEVELOPMENT AND PUBLISHING
UPDATE NOTICE

DELUA User's Guide

EK-DELUA-UG-CN1

December 1987

INSTRUCTIONS

Attach this update to the inside front cover of the *DELUA User's Guide*, and write the following corrections in ink.

Page	Correction
5-5	On Figure 5-5, delete the sixth block from the top. It currently reads, "PAD/1 BYTE."
5-6	In Table 5-1, delete the line that is the sixth field entry from the top. It currently reads, "PAD 1 The constant 0."

EK-DELUA-UG-002

Networks · Communications

DELUA User's Guide

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

TABLES

TABLES (Cont)

CHAPTER 1
INTRODUCTION

The DIGITAL Ethernet large-scale-integration UNIBUS adapter (DELUA) is an Ethernet communications controller option for VAX and PDP-11 computers.

The DELUA adapter is a follow-on product to the DIGITAL Ethernet UNIBUS network adapter (DEUNA). The DELUA option performs all the same functions as the DEUNA option, but it offers higher performance and lower power consumption.

NOTE

For ease of use and reader comprehension, the DELUA adapter will be referred to as the DELUA throughout the document. Similarly, the DEUNA adapter will be referred to as the DEUNA and the UNIBUS bus as the UNIBUS.

1.1 ETHERNET OVERVIEW

The Ethernet is a local area network (LAN) that provides high-speed data transfer among computers and other digital devices within a moderately sized geographic area. It is intended for devices requiring brief bursts of high-speed data transfers, such as terminal access, distributed processing, and office automation.

The primary characteristics of Ethernet include:

- **Topology** – branching bus.
- **Medium** – shielded coaxial cable, Manchester-encoded digital baseband signaling.
- **Data Rate** – 10 million bits per second (maximum).
- **Maximum Separation of Nodes** – 2.8 kilometers (1.7 miles) on one LAN; several LANs can be connected with LAN Bridge 100 devices to form an extended LAN.
- **Maximum Number of Nodes** – 1,024 nodes on one LAN; several LANs can be connected with LAN Bridge 100 devices to form an extended LAN.
- **Network Control** – multiaccess, fair distribution to all nodes.
- **Access Control** – carrier sense, multiple access with collision detect (CSMA/CD).
- **Frame Length** – 64 to 1518 bytes, including a data field from 46 to 1500 bytes.

The Ethernet is a medium-sized network. It is smaller than long-distance, low-speed networks that carry data for hundreds or thousands of kilometers and it is larger than specialized high-speed interconnections that are generally limited to tens of meters.

An example of a large-scale Ethernet configurations is shown in Figure 1-1. When configuring an Ethernet local area network you must observe the following rules:

1. A segment of coaxial cable can be a maximum of 500 meters (1640 feet) long. Each segment must be terminated at both ends with the characteristic impedance.

2. Up to 100 nodes can be connected to any segment of the cable. Nodes on a cable segment must be spaced at least 2.5 meters (8.2 feet) apart.

3. The maximum length of the transceiver cable between a transceiver and a controller, such as the DELUA, is 50 meters (164 feet). In the case of the DELUA, the internal cabling between the DELUA and its bulkhead assembly accounts for 10 meters (33 feet). The DELUA, therefore, can support up to 40 meters (131 feet) of transceiver cable.

4. The maximum length of coaxial cable between any two nodes in a single LAN is 1500 meters (4922 feet). However, the length of cable between two nodes can be greater if part of the cable is fiber-optic cable connected by repeaters. Also, this 1500-meter length limitation does not apply to nodes on different LANs of an extended LAN connected by LAN Bridge 100 devices.

5. A LAN can be extended by connecting two segments with repeaters and a length of fiber-optic cable. A fiber-optic cable connected to a repeater can be up to 1000 meters (3280 feet) long.

6. A maximum of two repeaters can be placed between any two nodes on the same LAN.

7. LAN Bridge 100 devices can be used to connect LANs to form an extended LAN. There is no limit to the number of LANs that can be connected using LAN Bridge 100 devices, but performance may be poor if a message must travel through more than seven bridges before reaching its destination node.

8. LAN Bridge 100 devices can be connected using a fiber-optic cable. The maximum length of such a cable depends on the type of cable and the number of splices and connectors, but it can extend as far as 2000 meters (6560 feet).

1.2 PHYSICAL DESCRIPTION

The DELUA is illustrated in Figure 1-2. The DELUA consists of:

- M7521 hex-height module
- UNIBUS Network Adapter (UNA) bulkhead assembly
- UNA bulkhead cable assembly

The DELUA kit for non-FCC-compliant cabinets (CK-DELUA-KI) also contains a bulkhead frame (74-27292-01).

The UNA bulkhead assembly is connected to the transceiver on the LAN's coaxial cable with a transceiver cable.

DELUA controls and indicators consist of two dual in-line package (DIP) switches and eight light-emitting diodes (LEDs) mounted on the M7521 module, plus an LED on the UNA bulkhead assembly. The switches are used to select DELUA operating parameters and are set before installing the module. The LEDs display DELUA selftest error and status information. The function of these switches and indicators is described in Chapter 2.

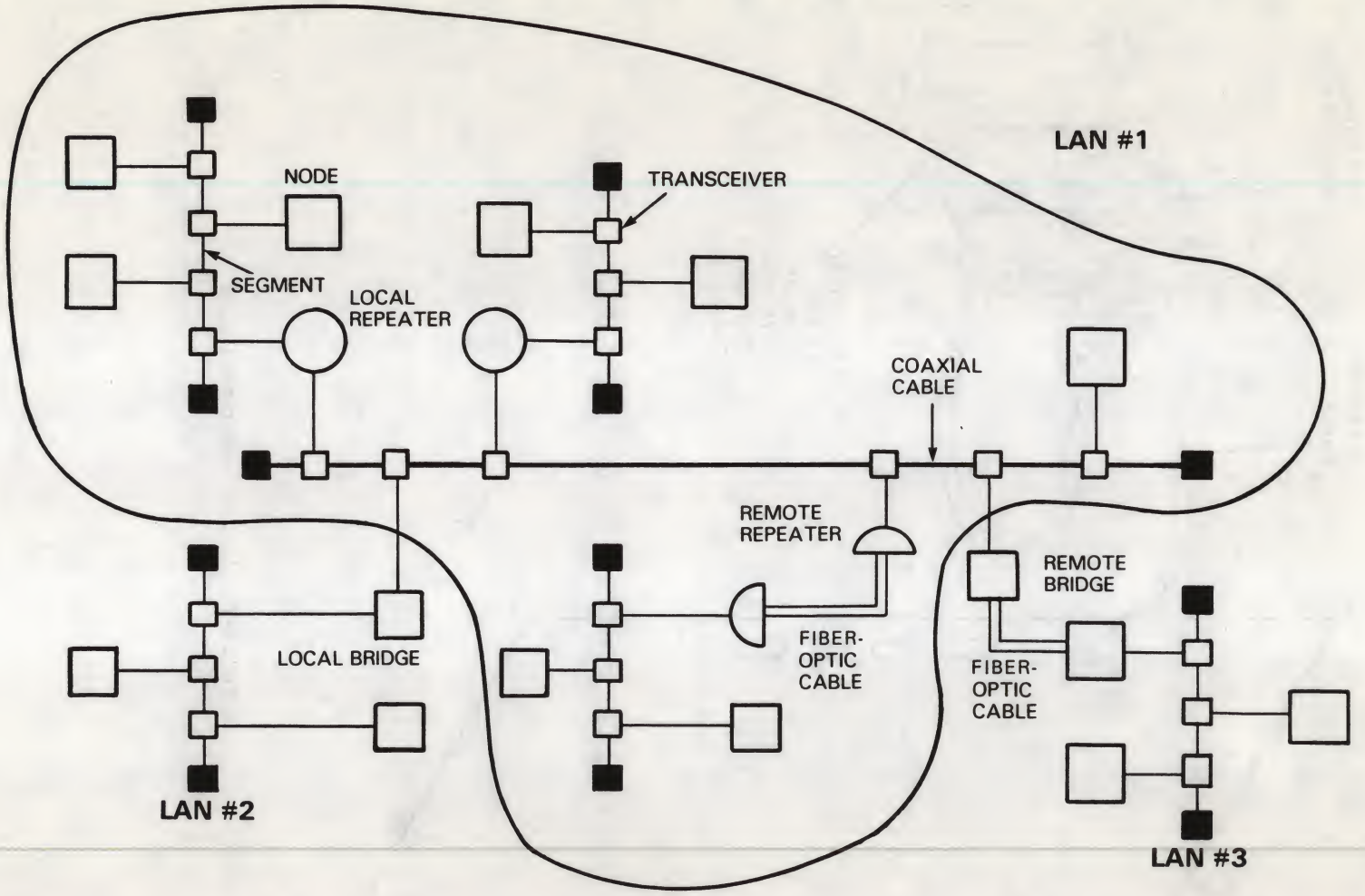

Figure 1-1 Large-Scale Ethernet Configuration

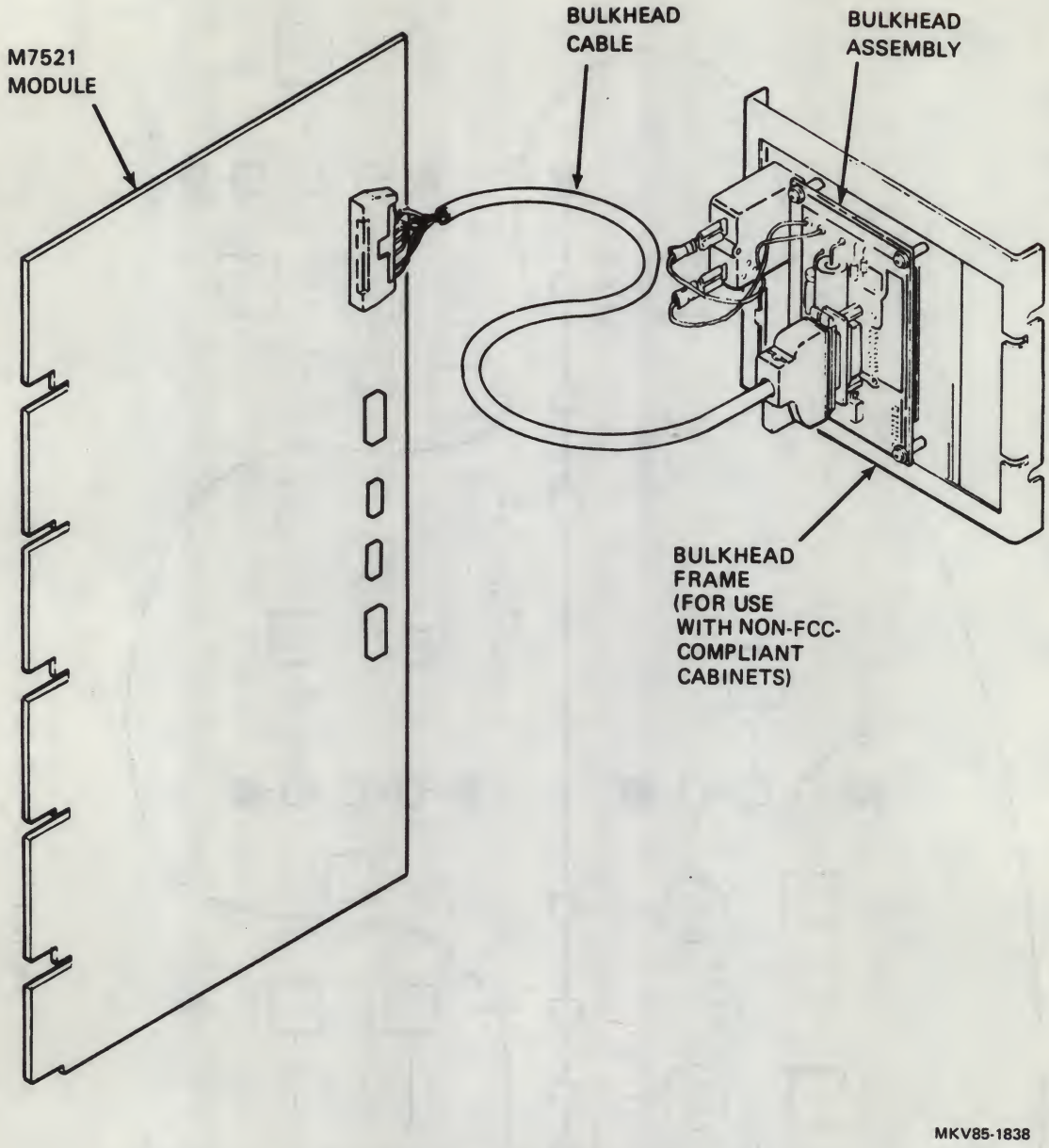

Figure 1-2 DELUA Component Parts

1.3 DELUA SYSTEM OPERATION

The DELUA controller performs both the data link layer functions and a portion of the physical channel functions. It also provides the following network maintainability functions:

- Loops back maintenance messages from other nodes
- Periodically transmits system identification
- Loads and boots its host operating system (PDP-11 only) from another node on the network

The DELUA provides all of the logic necessary to connect VAX and PDP-11 computers to a local area network (Figure 1-3). The DELUA performs data encapsulation and decapsulation, data link management, and all channel access functions to ensure maximum throughput with minimum host processor intervention.

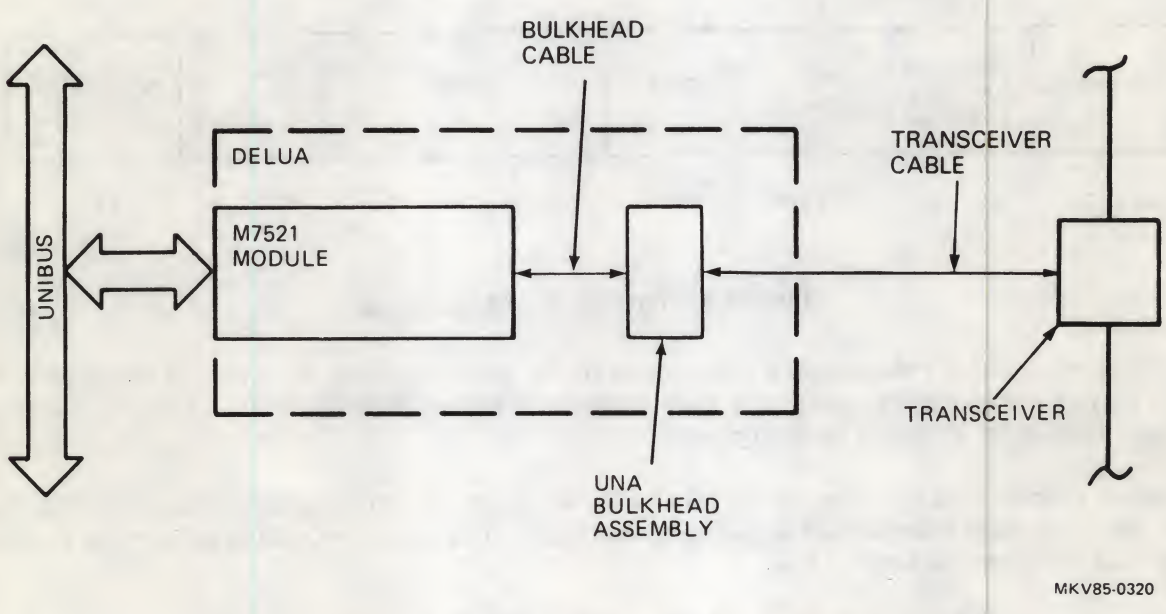

Figure 1-3 DELUA-to-LAN Block Diagram

1.3.1 Physical Channel Functions

The DELUA provides the following specific physical channel functions to interface with the transceiver:

During Transmission

- Generates the 64-bit preamble for synchronization
- Provides parallel-to-serial conversion of the frame
- Generates the Manchester encoding of data
- Ensures proper channel access by monitoring the presence of another station's transmission
- Monitors the selftest collision detect signal from the transceiver

During Reception

- Senses for presence of a carrier from another station
- Performs Manchester decoding of the incoming data stream
- Synchronizes itself to the preamble and removes the preamble before processing
- Provides serial-to-parallel conversion of the frame
- Buffers received frames

1.3.2 Data Link Layer Functions

The DELUA provides the following data link layer functions:

- Calculates the 32-bit cyclic redundancy check (CRC) value and sends it with the frame
- Attempts retransmission upon detecting a collision
- Checks incoming frames for the proper CRC value
- Accepts only frames with specified destination addresses

1.3.3 Data Encapsulation

The frame format is shown in Figure 1-4. Each frame begins with a 64-bit preamble that allows the receiving node to synchronize exactly to the data rate. Frames are separated by at least 9.6 μs to allow another node the opportunity to send a message.

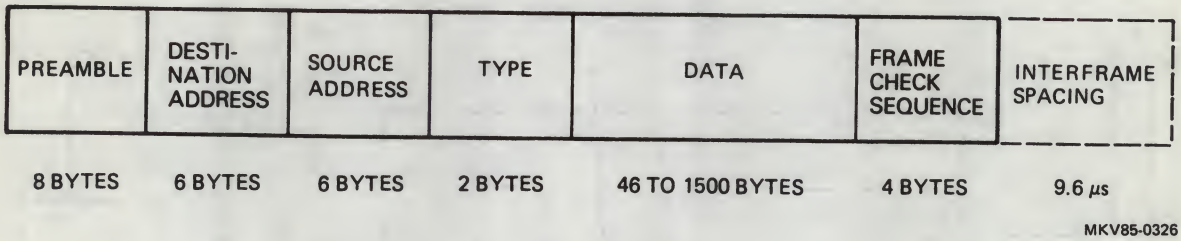

Figure 1-4 Format of a Data Frame

The destination address field contains the address of the node to which the frame is being sent. This address may be the address of a particular node, a multicast address associated with a group of nodes, or a broadcast address for all nodes on the network.

The source address field specifies the physical address of the transmitting node. Each DELUA has a unique 48-bit physical address built in during manufacture. The system software can override this value and assign a different physical address.

The type field is used by high-level network protocols. It indicates how the data field is to be interpreted.

The data field may have between 46 and 1500 bytes of data. The DELUA can be initialized to automatically insert null characters, if the amount of data is less than the minimum 46-byte data size.

The frame check sequence field contains a 32-bit CRC value, which is determined and inserted by the DELUA during transmission.

1.3.4 Data Decapsulation

The DELUA continuously monitors the signals received by its transceiver. After sensing a carrier, the DELUA uses the preamble sequence of the frame to synchronize itself to the data rate of the frame. The DELUA then processes the destination address field through a hardware comparator to determine whether the incoming frame is intended for its node. The DELUA accepts only frames that have a destination address matching one of the following types of addresses:

- The physical address of the node
- The broadcast address for all nodes
- One of the ten multicast group addresses that the user may assign to the DELUA, when desired
- Any multicast address, when desired
- All addresses, when desired

The DELUA performs a hardware comparison of the 6-byte destination address to determine if there is a match with the node's physical address or one of the user-designated multicast addresses. If the user desires to receive more than ten multicast address groups, then all multicast addresses can be passed to higher-level software for discrimination.

To assist in network management functions and to aid in fault diagnosis, the DELUA may operate in a mode that disregards the address field, thus accepting all frames received from the network. The DELUA verifies the integrity of the received data by recalculating the 32-bit CRC value and comparing it to the CRC obtained from the received frame.

1.3.5 Link Management

The method used for channel access is called carrier-sense, multiple-access with collision-detection (CSMA/CD). The DELUA controls all of the link management functions necessary to send or receive a frame of data. These functions include:

- **Carrier Deference** – The DELUA monitors the physical channel for traffic. If the channel is busy, the DELUA waits until it is not busy before sending a frame.

- **Collision Detection** – Collisions occur when two or more controllers attempt to transmit data simultaneously on the channel. The DELUA monitors the collision sense signal generated by a transceiver to detect a collision. When it detects a collision, it continues to transmit for a period of time to ensure that all other nodes detect the collision.

- **Collision Backoff and Retransmission** – When a controller attempts a transmission and encounters a collision on the channel, it attempts a retransmission a short time later. The schedule for retransmission is determined by a controlled randomization process called truncated binary exponential back-off. The DELUA attempts to transmit a total of 16 times (15 times plus the original transmission). If it fails after these 16 tries, it will report an error.

1.4 DIAGNOSTIC FEATURES

Microdiagnostics, system, and network diagnostics are used to minimize the time required to isolate and diagnose a network communication fault. Built-in selftest microdiagnostics automatically test the DELUA component logic during powerup. These selftest diagnostics report errors by means of LEDs on the edge of the module.

To eliminate the possibility that the DELUA may monopolize the network after certain logic failures, the DELUA has a special circuit that limits the frame transmit period.

The DELUA monitors the transceiver's collision test signal after every frame transmission to verify that the collision sense circuitry is working properly.

At the request of another node, the DELUA sends a loopback message to the node specified by the requesting node. This feature allows physical connections between nodes to be verified.

The DELUA detects and tabulates network statistics and error conditions for use by higher-level network management applications.

1.5 INTERNAL HARDWARE OVERVIEW

The DELUA is a microprocessor device based on the Motorola 68000™ microprocessor. The internal hardware of the DELUA is divided into the following major subsystems also shown in Figure 1-5.

- Microprocessor
- Memory
- Local Area Network Controller for Ethernet (LANCE)
- Direct Memory Access (DMA)
- Port Control and Status Registers

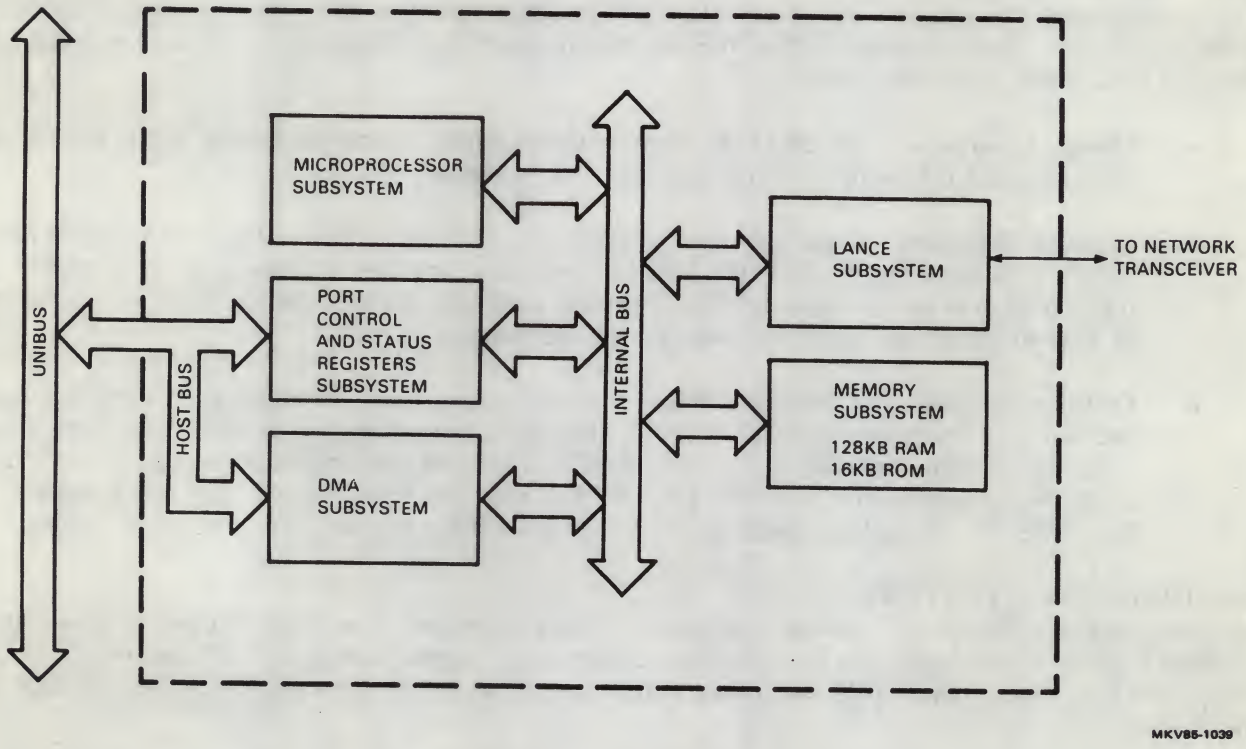

Figure 1-5 DELUA Block Diagram

1.5.1 Microprocessor Subsystem

The Motorola 68000 microprocessor has a 400 ns cycle time and supports auto-vectored interrupts. Each of the internal subsystems has its own interrupt vector address. The microprocessor also resolves internal bus (IBUS) arbitration conflicts when two or more internal subsystems try to use the IBUS simultaneously.

1.5.2 Memory Subsystem

The internal memory is made up of 128K bytes of random access memory (RAM) used for data buffering and microcode execution, and 16K bytes of ROM containing the microcode. There is also an 8-byte ROM containing the Ethernet physical address assigned to the DELUA during manufacturing.

During powerup the DELUA copies its microcode from ROM to RAM because the memory cycle time of RAM is faster.

Motorola 68000 is a trademark of Motorola, Inc.

The memory control and status register provides the microprocessor with status information on memory errors and allows the microprocessor to remap memory at powerup. This register also allows the microprocessor to disable parity checking and force parity errors for microdiagnostic purposes. Normally, the left byte of each word has even parity and the right byte has odd parity. Thus, a failure that produces data of all ones or all zeros will produce a parity error.

The system timer circuit causes a 300 ns memory refresh cycle every 8 μs.

1.5.3 LANCE Subsystem

The LANCE itself is also a microprocessor-controlled device. When the DELUA is initialized, the DELUA microprocessor provides the LANCE with receive data buffers in DELUA internal memory. The LANCE watches message traffic on the network and checks the destination address of each frame. If the address matches the DELUA physical address, a multicast address, or the broadcast address, the LANCE writes the frame into one of the receive data buffers and interrupts the microprocessor. The LANCE checks the CRC field of the frame and reports any errors to the microprocessor.

When the microprocessor has a frame to send on the network, it writes an entry in the LANCE transmit descriptor ring in DELUA memory and then sets the transmit demand bit in the LANCE control and status register 0. The LANCE waits until there is a pause in the message traffic on the network and then sends the frame. The LANCE adds the preamble and CRC fields to the frame as it sends it. If the frame collides with a frame from another node, the LANCE waits and then tries again (up to 16 tries). After sending the frame, the LANCE writes status into the transmit descriptor ring entry in DELUA memory and interrupts the microprocessor.

The LANCE mode register provides a number of special features for diagnostic testing. The LANCE can loop data frames inside the LANCE subsystem or out onto the network cable and back. It can force a collision to test the collision detection circuitry. It can also disable the CRC generation circuitry. This allows a diagnostic test to send frames with correct and incorrect CRC fields to test the LANCE CRC detection circuitry.

1.5.4 Direct Memory Access (DMA) Subsystem

The DMA subsystem transfers data between DELUA memory and host memory. The DMA subsystem comprises a word mover and a block mover. The word mover transfers one word from host memory to DELUA memory, or from DELUA memory to host memory. The block mover transfers a block of contiguous words. The word mover and the block mover can operate simultaneously.

The microprocessor uses the word mover to read ancillary functions, addresses, and pointers from host memory and to write status words into host memory. It uses the block mover to write frames it has received on the network into host memory and to read frames from host memory to transmit on the network.

To transfer a word or a block of words between internal memory and host memory, the microprocessor writes registers in the DMA subsystem to specify the internal memory address, the host memory address, the number of words to be transferred, and the direction of transfer. The DMA subsystem interrupts the microprocessor when the transfer is complete.

1.5.5 Port Control and Status Register (PCSR) Subsystem

The DELUA has four port control and status registers for communication with the host. Inside the DELUA, the microprocessor has direct access to only PCSR0. PCSR1, PCSR2, and PCSR3 are not connected to the internal bus. The microprocessor uses the DMA word mover to read and write these registers by way of the UNIBUS.

1.6 SPECIFICATIONS

Table 1-1 lists the DELUA specifications.

Table 1-1 DELUA Specifications

Specification	Description
Operating Mode	Half-duplex
Data Format	Ethernet specification
Data Rate (Physical Channel)	10M bits/sec
UNIBUS Loading	1 dc load 4 ac loads
DC Power Requirements	+5 ±0.25 V, 8 A −15 V, 1 A (for transceiver)
Physical Size	
M7521 Module	Height (hex): 21.4 cm (8.4 in) Length: 39.8 cm (15.7 in)
Bulkhead Assembly	Height: 10.6 cm (4.0 in) Length: 10.6 cm (4.0 in)
Operating Environment	
Temperature	10° to 50°C (50° to 122°F)
Relative Humidity	10% to 90% (noncondensing)
Wet-Bulb Temperature	28°C (82°F) maximum
Dew Point	2°C (36°F)
Altitude	Sea level to 2.4 km (8000 ft)
Shipping Environment	
Temperature	−40°C to 66°C (−40 to 151°F)
Rate of Change	20°C/hr (36°F/hr) maximum
Relative Humidity	0% to 95% (noncondensing)
Altitude	Sea level to 9 km (30,000 ft)

1.7 RELATED DOCUMENTS

Table 1-2 lists related documents.

Table 1-2 Related Documents

Title	Order Number
DELUA Technical Description	EK-DELUA-TD
H4000 Technical Description	EK-H4000-TM
The Ethernet, A Local Area Network, Data Link Layer, and Physical Layer Specifications	AA-K759B-TK
Ethernet Installation Guide	EK-ETHER-IN
Network Interconnect Exerciser User's Guide	AA-HI06A-TE
Introduction to Local Area Networks	EB-22714-XX
DELUA Maintenance Print Set	MP-01787-01

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CHAPTER 2
INSTALLATION

This chapter provides the information necessary for installing a DELUA in a PDP-11 or VAX host system.

2.1 PREINSTALLATION CONSIDERATIONS

The following factors should be considered before installing a DELUA:

- Backplane requirements
- Bus latency constraints
- Bus loading factor

2.1.1 Backplane Requirements

The DELUA requires one hex-height, small peripheral controller (SPC) slot that can be configured for nonprocessor request (NPR) operations. Any SPC backplane [DD11-B (REV E) or later] can accept a DELUA module. The DELUA module can be placed anywhere on the UNIBUS system, but before all UNIBUS repeaters.

2.1.2 Bus Latency Constraints

For the DELUA, bus latency is the delay between the time the DELUA raises the nonprocessor request (NPR) UNIBUS signal line and the time it receives the nonprocessor grant (NPG) signal, which allows it to transfer a word on the UNIBUS. Excessive bus latency will slow the DELUA when it is reading and writing words from the host processor's memory using direct memory access (DMA). Since the DELUA is a very well-buffered device, it is unlikely to lose data due to excessive bus latency.

A module in a UNIBUS backplane slot closer to the processor has a higher NPR priority and, thus, a lower bus latency. To obtain optimum DELUA performance, select a backplane slot that places the DELUA module before all devices with a lower NPR rate and before all UNIBUS repeaters. If optimum performance is not a requirement, the DELUA module can be installed anywhere on the UNIBUS before all repeaters.

2.1.3 Bus Loading Factor

Make sure that system loading capacities are not exceeded as a result of installing the DELUA. The DELUA ac and dc loads on the UNIBUS signal lines are as follow:

- UNIBUS dc loads – 1
- UNIBUS ac loads – 4

The power consumption of the DELUA is shown in Table 2-1.

Table 2-1 DELUA Power Consumption

Power Supply	Allowable Range	Current	Backplane Pin
+5 V	+4.75 V to 5.25 V	8 A	CA2
−15 V (for transceiver)	−14.25 V to −15.75 V	1 A	FB2

2.2 UNPACKING AND INSPECTION

To unpack a DELUA subsystem, remove the equipment from its shipping containers, verify that there are no missing parts, and inspect the equipment for damage. Report any damage or shortages to the shipper and notify the DIGITAL representative.

1. Before opening the shipping containers, check for external damage such as dents, holes, or crushed corners.

CAUTION

The M7521 module and the UNA bulkhead assembly are easily damaged by static electricity. To avoid damage, handle these parts only on the Velostat™ mat. When not in use, store these parts in their conductive plastic bags.

2. Open a Velostat static discharge system (CD kit no. A2-W0299-10) and unfold the mat.

3. Attach one end of the 4.5-meter (15-foot) ground cable to an electrical ground point in the host computer. Attach the other end to the mat snap fastener.

4. Attach the wrist strap to your wrist and clip the other end of the cable to the edge of the mat.

5. Open and unpack the shipping container. Check the contents against the parts shown in Figure 2-1.

NOTE

Keep the packing materials in case you must return parts.

6. Inspect each part for shipping damage. Check the modules carefully for cracks, breaks, or loose components, such as socketed chips.

2.3 PREINSTALLATION PREPARATION

To prepare the DELUA for installation, perform the steps described in Sections 2.3.1 through 2.3.5.

Velostat is a trademark of the 3M Company.

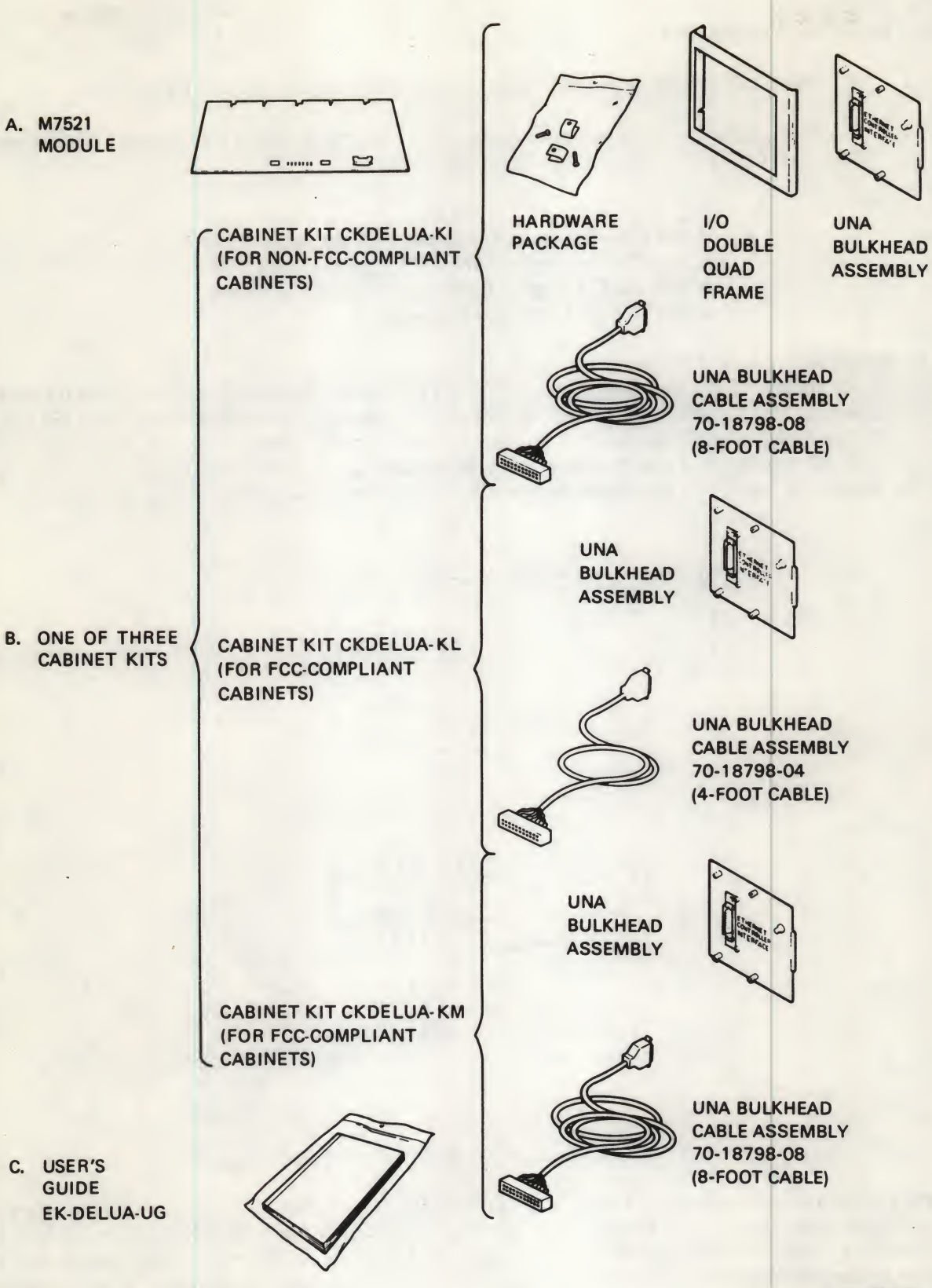


Figure 2-1 DELUA Component Parts

2.3.1 Backplane Preparations

1. If present, remove the grant continuity module from the slot for the DELUA.

2. If present, remove the nonprocessor grant (NPG) jumper wire that runs between backplane pins CA1 and CB1 of the slot for the DELUA module.

NOTE

If at a later time you remove the DELUA module, be sure to either replace the NPG jumper wire and install a G727 single-height grant module, or install a G7273 dual-height grant module.

2.3.2 Device Address Assignment

Set the device address of the first DELUA (or DEUNA) being installed in a system to 774510 by setting the switch pack at E106 as shown in Figure 2-2. For device address assignment purposes, the DELUA and the DEUNA are equivalent. The DELUA address of 774510 could overlap with the twenty-third DP11 (double-buffered synchronous line controller) if your system has 23 DP11 controllers. If it does, select another address for the DP11 controller from the floating address space described in Appendix A.

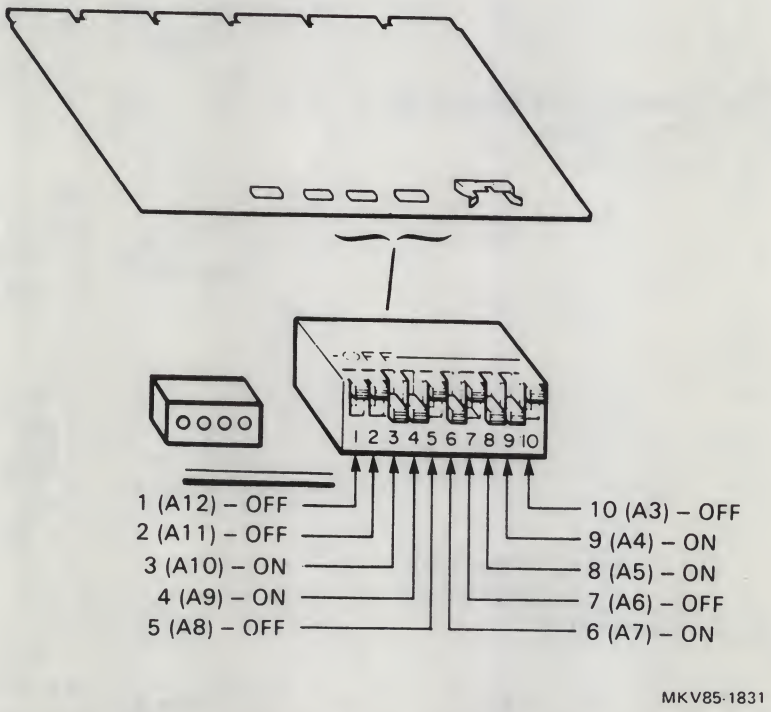


Figure 2-2 Switch Pack at E106, Device Address Assignment

For the second and any subsequent DELUA (or DEUNA) being installed in the same system, select the device address from the floating address space. If the system already has a DEUNA, select the DELUA device address from the floating address space. Figure 2-3 shows the correlation between address bits and switches in the switch pack at E106. Refer to Appendix A for information on determining the appropriate floating address.

MSB LSB

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	SWITCH PACK E106										0	0	0

SWITCH NUMBER	1	2	3	4	5	6	7	8	9	10	FLOATING ADDRESS
										OFF	760010
									OFF		760020
									OFF	OFF	760030
								OFF			760040
								OFF		OFF	760050
								OFF	OFF		760060
								OFF	OFF	OFF	760070
							OFF				760100
						OFF					760200
						OFF	OFF				760300
					OFF						760400
					OFF		OFF				760500
					OFF	OFF					760600
					OFF	OFF	OFF				760700
				OFF							761000
			OFF								762000
			OFF	OFF							763000
		OFF									764000

MKV85-1836

Figure 2-3 Device Address and Switch Positions

2.3.3 Vector Address Assignment

Set the vector address of the first DELUA (or DEUNA) being installed in a system to 120 by setting the switch pack at E69, as shown in Figure 2-4. For vector assignment purposes, the DELUA and the DEUNA are equivalent.

For the second and any subsequent DELUA (or DEUNA) being installed in the same system, select the vector address from the floating vector address space. If the system already has a DEUNA, select the DELUA vector address from the floating vector address space. Figure 2-5 shows the correlation between vector address bits and switches in the switch pack at E69. Refer to Appendix A for information on determining the appropriate floating address.

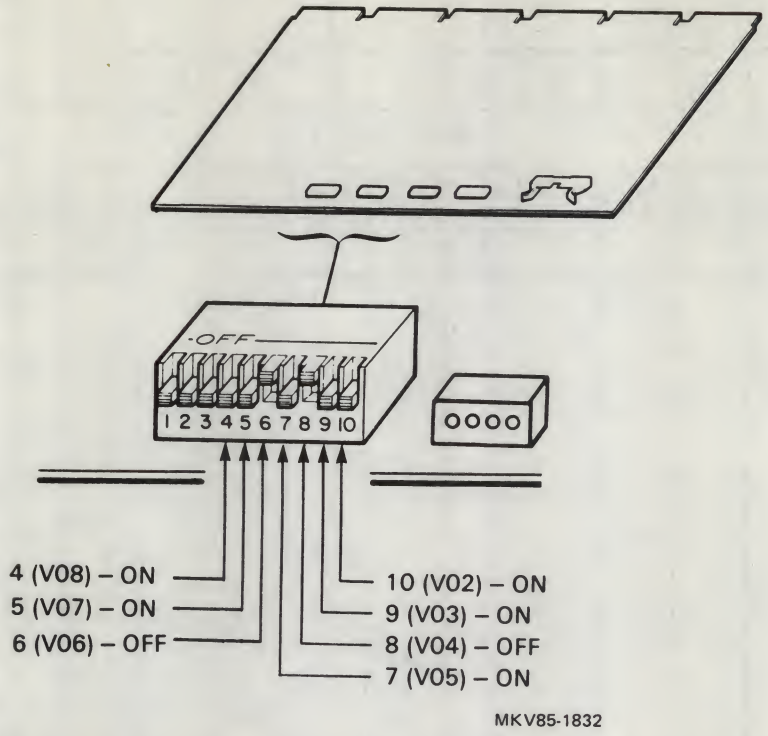


Figure 2-4 Switch Pack at E69, Vector Address Assignment

FLOATING VECTOR ASSIGNMENT TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	SWITCH PACK E69						0	0

SWITCH NUMBER	4	5	6	7	8	9	10	FLOATING VECTOR
		OFF	OFF					300
		OFF	OFF				OFF	304
		OFF	OFF			OFF		310
		OFF	OFF			OFF	OFF	314
		OFF	OFF		OFF			320
		OFF	OFF		OFF		OFF	324
		OFF	OFF		OFF	OFF		330
		OFF	OFF		OFF	OFF	OFF	334
		OFF	OFF	OFF				340
		OFF	OFF	OFF			OFF	344
		OFF	OFF	OFF		OFF		350
		OFF	OFF	OFF		OFF	OFF	354
		OFF	OFF	OFF	OFF			360
		OFF	OFF	OFF	OFF		OFF	364
		OFF	OFF	OFF	OFF	OFF		370
		OFF	OFF	OFF	OFF	OFF	OFF	374
	OFF							400
								- - -
	OFF		OFF					500
								- - -
	OFF	OFF						600
								- - -
	OFF	OFF	OFF					700
								- - -

MKV85-1833

Figure 2-5 Vector Address and Switch Positions

2.3.4 Boot Option Selection (PDP-11 Host Systems Only)

At the request of another node, a DELUA installed in a PDP-11 host can load the host operating system. Switch settings on the DELUA module determine whether the DELUA loads the host by transferring the operating system software across the network from another node, or signals the host to load itself from its own mass storage system. The DELUA cannot load a VAX host.

The DELUA can be set up to perform a remote boot on powerup with the optional M9312 boot module and ROM set, order number MR11K-AE. During powerup, the DELUA loads the host operating system by transferring the operating system software across the network from another node.

When installing a DELUA into a PDP-11 host system, set switches 2 and 3 of the switch pack at E69 for the boot function desired. Figure 2-6 shows switches 2 and 3. Table 2-2 lists the switch settings and boot functions. Section 5.1 provides additional information on remote boot functions.

When installing a DELUA into a VAX host system, set switches 2 and 3 on the switch pack at E69 to the ON (disabled) position. Figure 2-6 shows switches 2 and 3.

Table 2-2 Boot Function Switches (PDP-11 Only)

Switch 2	Switch 3	Boot Function
ON	ON	Remote boot disabled
ON	OFF	Remote boot from system boot ROM
OFF	ON	Remote boot and system load
→ OFF	OFF	Remote boot disabled

2.3.5 Loop Selftest Switch (for Manufacturing Use)

Disable the loop selftest feature by setting switch 1 on the switch pack at E69 to the ON position as shown in Figure 2-7.

Enabling the loop selftest feature does not cause the selftest to start, but once it is started (such as by a powerup) the selftest will loop continuously.

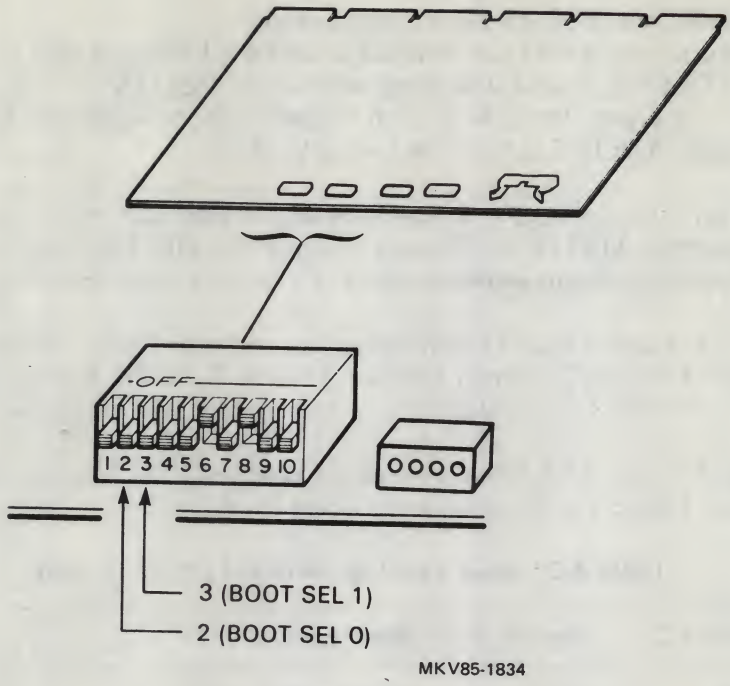


Figure 2-6 Boot Function Switches

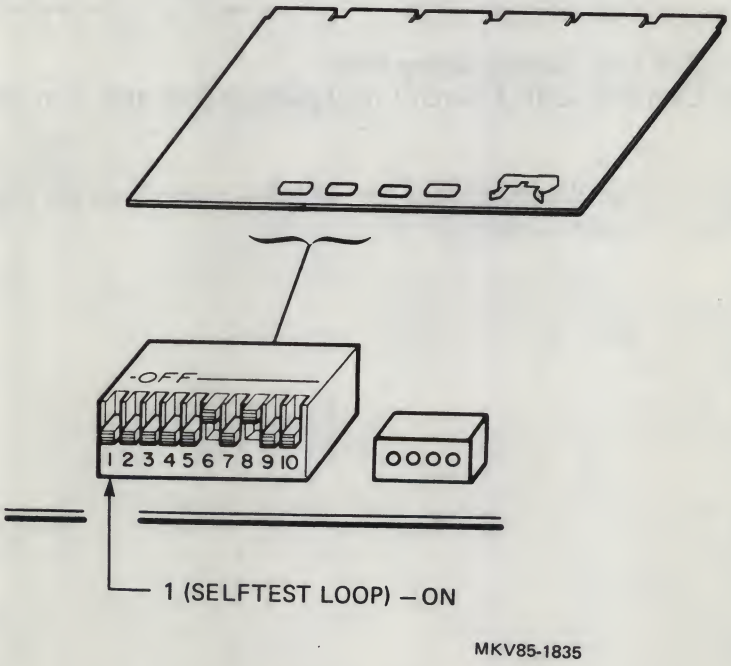
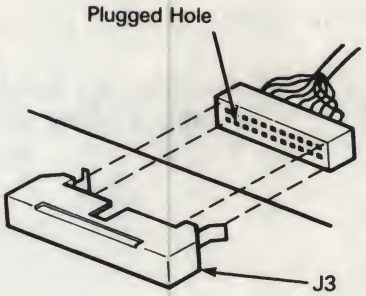


Figure 2-7 Loop Selftest Switch Setting

2.4 INSTALLATION

Perform the steps shown in Figure 2-8 to install the DELUA.

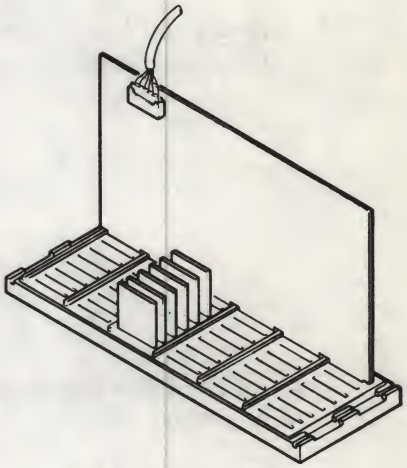
1. **Install the UNA bulkhead cable.** Note the plugged hole in the Berg™ connector on the UNA bulkhead cable. Plug the connector into J3 on the DELUA module.



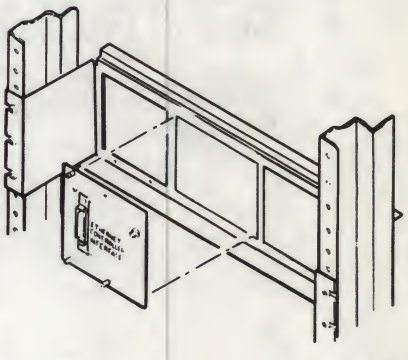
2. **Install the DELUA module.** Install the DELUA (M7521) module in the selected backplane slot.

NOTE

Remove the NPR jumper (CA1 to CB1) before installing the DELUA module. You must reinstall this jumper if you remove the DELUA module from the system.



3. **Install the UNA bulkhead (FCC-compliant bulkhead panel).** Remove the blank bulkhead panel and install the UNA bulkhead assembly.



MKV85-1839

Figure 2-8 DELUA Installation Procedure (Sheet 1 of 2)

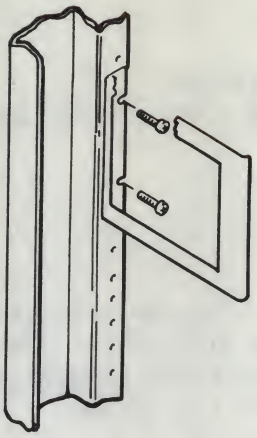
Berg is a trademark of Berg Electronics.

4. Install the UNA bulkhead (non-FCC-compliant bulkhead panel).

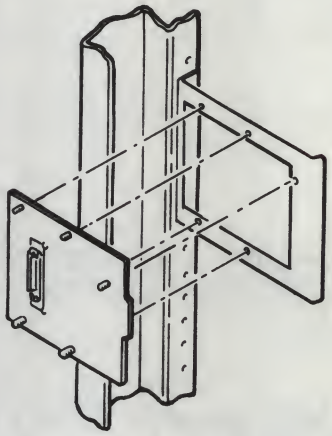
a. Locate the two 10-32 screws and u-nuts.

b. Slip the u-nuts onto the cabinet frame.

c. Secure the I/O bulkhead metal frame to the cabinet frame.



d. Install the UNA bulkhead assembly into the metal frame.



5. Connect the UNA bulkhead cable to the bulkhead assembly.

a. Unlock the latch on the cable D connector.

b. Connect the cable to J2 on the component side of the UNA bulkhead assembly.

c. Slide the latch on the D connector to the locked position.

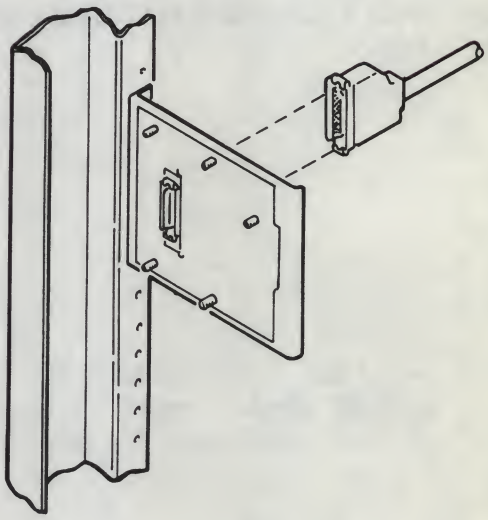


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Figure 2-8 DELUA Installation Procedure (Sheet 2 of 2)

2.5 VERIFICATION CHECKS

Perform the following tests to verify that the DELUA is operating correctly.

For these tests the DELUA must be attached to the network or to an H4080 loopback transceiver as shown in Figure 2-9. The H4080 loopback transceiver is not included with the DELUA.

NOTE

DIGITAL personnel may obtain the H4080 loopback transceiver through their local DIGITAL Field Service branch office. Customers may obtain the H4080 through their local DIGITAL Sales Representative.

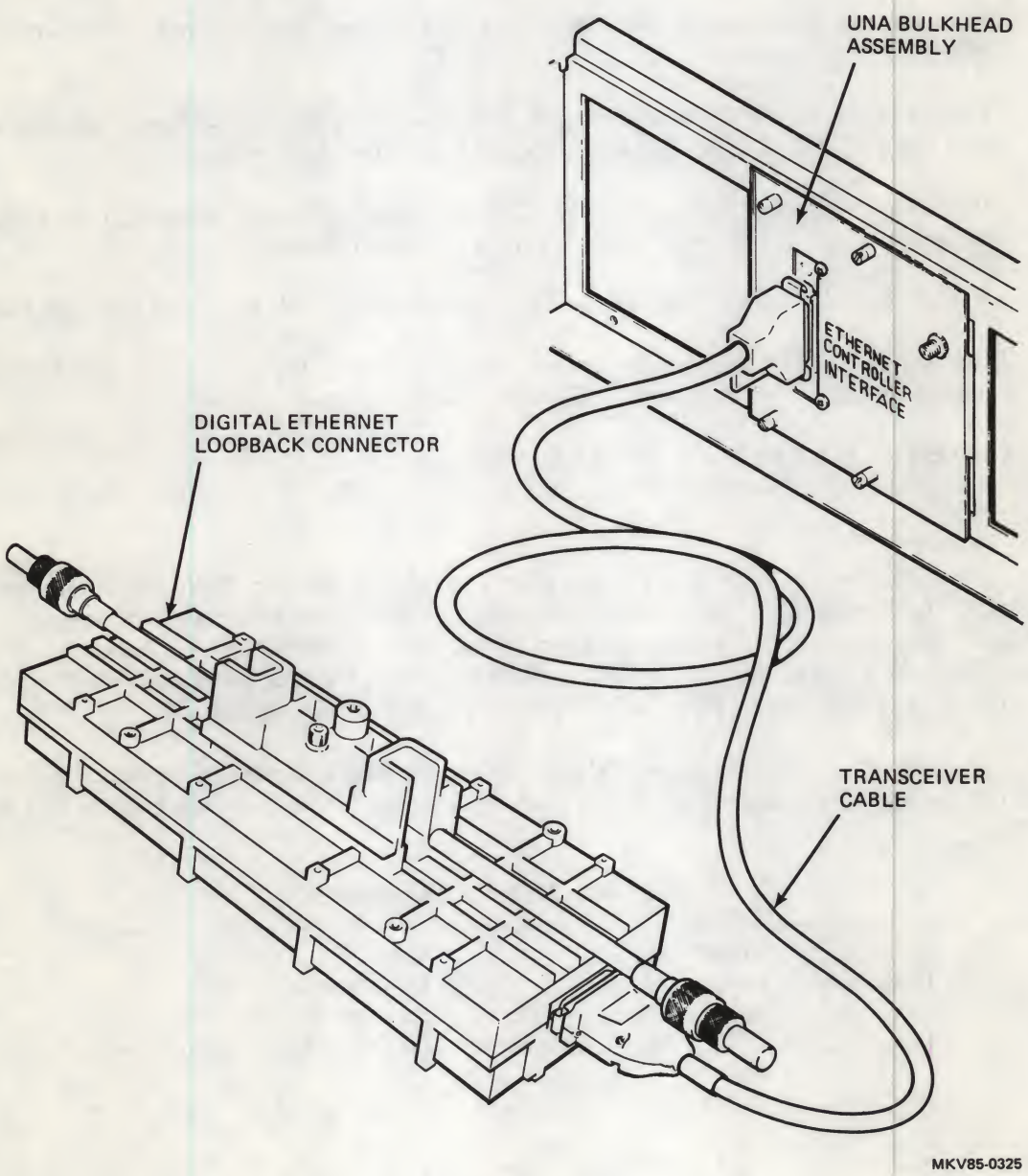


Figure 2-9 Loopback Transceiver Setup

2.5.1 Postinstallation Power Check

Turn on the system power and verify that the voltages at backplane pins CA2 and FB2 are in accordance with those listed in Table 2-3. If necessary, adjust the power supply voltages.

Table 2-3 DELUA Power Check

Power Supply	Allowable Range	Backplane Pin
+5 V	+4.75 V to 5.25 V	CA2
−15 V (for transceiver)	−14.25 V to −15.75 V	FB2

2.5.2 Light-Emitting Diode (LED) Checks

1. Turn on the system power. Note that the DELUA must be connected to the network or to a loopback test transceiver.

2. The LEDs on the DELUA module will cycle indicating that the selftest diagnostic is running (see Figure 2-10). The selftest takes about 15 seconds to complete.

   When the test completes successfully, LED D8 should be on indicating that the DELUA is in the ready state. The activity LED, D5, may also be flickering.

   If any other LEDs are on, the selftest has found an error. Table 6-1 shows the LED status codes.

3. Check that the UNA bulkhead assembly LED shown in Figure 2-11 is lighted. This LED is lighted by the −15-volt power supply that powers the transceiver.

2.6 DIAGNOSTIC ACCEPTANCE PROCEDURE

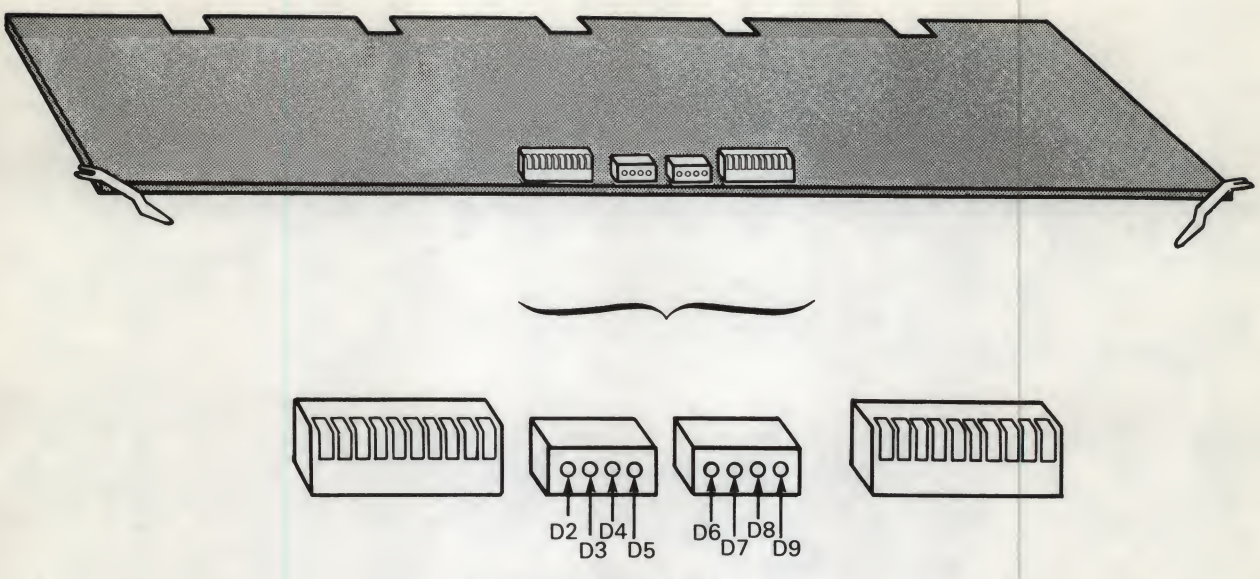
The final step in the DELUA installation procedure is to exercise the DELUA on the UNIBUS and on the network.

Run the appropriate diagnostics for the VAX or PDP-11 system as listed in Table 2-4. To run the PDP-11 diagnostics, CZUAD and CXUAD, the DELUA must be connected to a loopback transceiver. These diagnostic programs assume that the only messages to and from the transceiver are the messages they have sent. If the DELUA is connected to a network and the diagnostic receives a message sent by another node on the network, it reports errors. Run each diagnostic for at least five passes.

To run the network interconnect exerciser (NIE) program, the DELUA must be connected to the network. Refer to the *Network Interconnect Exerciser User's Guide* (order number AA-HI06A-TE) for further information.

Table 2-4 DELUA Diagnostics

Diagnostic	PDP-11 Host System	VAX Host System
Functional	CZUAD (Stand-Alone)	EVDYB (Level 2R On-Line)
DEC/X-11	CXUAD (Stand-Alone)	None
NIE	CZUAC (Stand-Alone)	EVDWC



NOTE: LED D2 IS NOT USED.

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Figure 2-10 DELUA LEDs

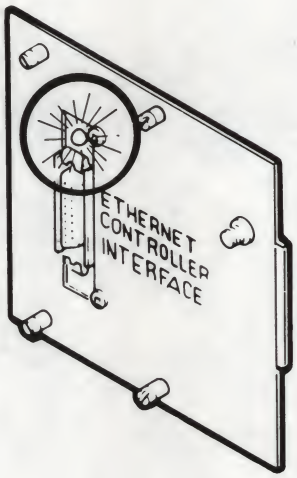

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Figure 2-11 Bulkhead LED

CHAPTER 3
PROGRAMMING OVERVIEW

3.1 INTRODUCTION

The operation of the DELUA is controlled by a program in host memory called the port driver. The port driver controls the DELUA in two ways: with port commands written to the four control and status registers, and by ancillary commands written into shared data structures in host memory. Figure 3-1 shows the DELUA control and status registers and the different data structures in host memory.

3.2 PORT COMMAND EXECUTION

Port commands are used to start and stop the DELUA, to tell it to read and execute an ancillary function in host memory, and to tell it to transmit a message on the network. The host processor issues a port command by writing bits ⟨03:00⟩ of the port control and status register 0 (PCSR0). The DELUA responds by executing the port command and setting the done interrupt (DNI) bit or the port command error interrupt (PCEI) bit.

3.3 ANCILLARY FUNCTION EXECUTION

The host processor issues an ancillary function by writing to a data structure in host memory called the port control block (PCB) rather than directly to PCSR0. The PCB consists of four 16-bit words in host memory.

Ancillary functions are used to read and write various addresses and pointers, and to read counters and extended status information in the DELUA.

When the DELUA is initialized, the port driver gives the DELUA the starting address of the PCB by writing a GET PCBB port command to PCSR0.

The following list shows a typical sequence of events when the DELUA executes an ancillary function:

1. The port driver writes (moves) the ancillary function to the PCB and, if necessary, sets up other memory data structures.

2. The port driver instructs the DELUA to fetch and execute the ancillary function by writing a GET COMMAND port command to PCSR0.

3. The DELUA uses direct memory access (DMA) to read the PCB and execute the ancillary function.

4. When the DELUA has finished, it notifies the host by setting the done interrupt (DNI) bit in PCSR0.

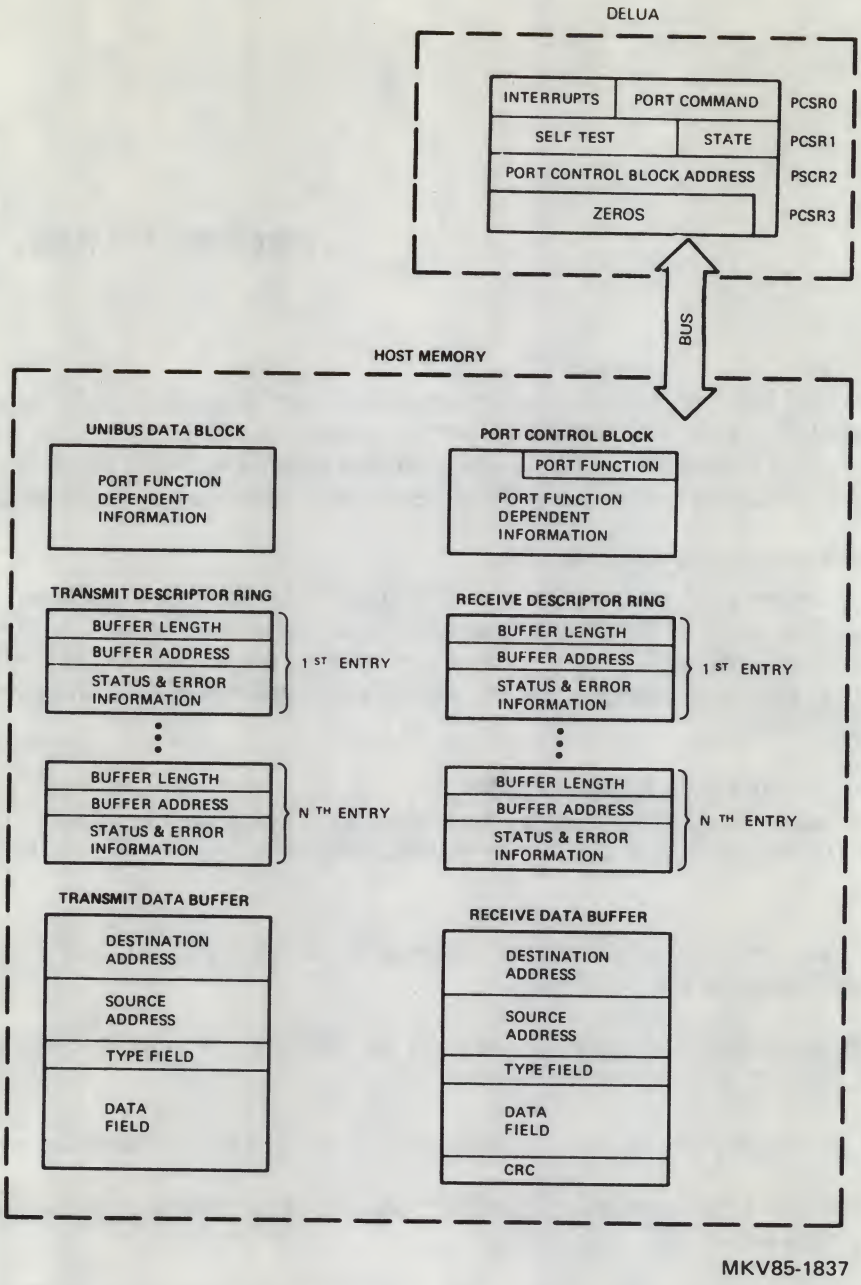


Figure 3-1 DELUA PCSRs and Host Memory Data Structures

3.4 DATA FRAME TRANSMISSION AND RECEPTION

The DELUA transmits and receives message frames directly between the network and the host's memory with DMA operations. The port driver tells the DELUA where to get frames to transmit and where to place frames it has received by means of transmit and receive descriptor rings in host memory.

The transmit descriptor ring contains a number of entries. Each entry specifies the length and starting address of a data buffer in host memory. If the ownership bit in one or more of the transmit descriptor ring entries is set, the DELUA reads the specified data buffers and transmits them on the network.

The receive descriptor ring also contains a number of entries. Each entry specifies the length and starting address of a receive data buffer in host memory. When the DELUA receives a frame on the network, it writes the frame into one of these receive data buffers.

When the host has frames for the DELUA to transmit, it writes an entry in the transmit descriptor ring for each frame. In each entry the host specifies the length and starting address of the transmit data buffer. The host also sets the ownership bit in the transmit descriptor ring entry. The host then writes the POLLING DEMAND port command into PCSR0. The POLLING DEMAND port command causes the DELUA to read the entries in the transmit descriptor ring. When the DELUA finds an entry with the ownership bit set, it transmits the contents of the data buffer as a frame on the network. The DELUA can also chain together the contents of several transmit data buffers into a single longer frame. If the end-of-frame bit in the descriptor ring entry is not set, the DELUA appends the next data buffer to form a longer frame. The DELUA continues appending data buffers into a single long frame until it encounters a descriptor ring entry with the end-of-frame bit set. After the DELUA has transmitted the frame, it writes status information into the transmit descriptor ring entry. The DELUA then continues to read entries in the transmit descriptor ring looking for more entries with the ownership bit set. After the DELUA has found all of the descriptor ring entries with the ownership bit set and transmitted the associated data buffers, it sets the transmit ring interrupt bit in PCSR0, which interrupts the host.

The host allocates receive data buffers for use by the DELUA by setting the ownership bit in each receive descriptor ring entry. When the DELUA receives a frame on the network, it writes the frame data into the next allocated receive data buffer. If the data buffer is not large enough to fit the entire frame, the DELUA fills successive receive buffers until it completes the frame. It sets the start-of-frame bit in the receive descriptor ring entry for the first buffer and it sets the end-of-frame bit in the receive descriptor ring entry for the last buffer. The DELUA clears the ownership bit in the receive descriptor ring entry and sets the receive interrupt bit in PCSR0, which interrupts the host.

3.5 FUNCTIONAL STATES

The DELUA reports its functional state with bits ⟨03:00⟩ of PCSR1. These states are described in Table 3-1.

Table 3-1 Functional States

Functional State	Description
Running	The DELUA enters the running state when it receives the START port command in PCSR0. When in the running state, the DELUA performs the following functions: • Transmits and receives frames on the network • Responds to port commands from the host • Maintains internal counters • Loops frames when requested by another node • Sends system ID frame • Accepts a remote boot frame from another node if the boot select switch is enabled

Table 3-1 Functional States (Cont)

Functional State	Description
Ready	The DELUA enters the ready state after powerup, remote boot, or after receiving a STOP port command. When in the ready state, it does not transmit or receive message frames, but it does perform the following functions: • Responds to port commands from the host • Maintains internal counters • Loops frames when requested by another node • Sends system ID frame • Accepts a remote boot frame from another node if the boot select switch is enabled
Reset	The DELUA enters the reset state during powerup, when it receives the UNIBUS initialization signal, or when the host sets the RESET bit in PCSR0. During the reset state, the DELUA clears its internal registers and counters. It also runs its selftest diagnostic if it has not already successfully run since the last powerup. If selftest is successful, the DELUA enters the ready state.
Primary Load	The DELUA enters the primary load state when it is requested to load the host operating system. This happens when the DELUA receives a BOOT port command in PCSR0 or a boot frame from another node. The DELUA transmits a request program frame and then waits for a memory load with transfer address frame from another node. The memory load with transfer address frame contains the secondary loader program that the DELUA loads into its internal memory. When in the primary load state, the DELUA also performs the following functions: • Maintains internal counters • Loops frames when requested by another node • Sends system ID frame • Accepts a remote boot frame from another node after it has been in the primary load state for 40 seconds or more
Secondary Load	The DELUA enters the secondary load state when the primary loader has loaded the secondary loader program from another node into DELUA internal memory. The secondary loader program loads a tertiary loader program from another node into host memory and starts it.

Table 3-1 Functional States (Cont)

Functional State	Description
Port Halted	The DELUA enters the port halted state when it receives a HALT port command in PCSR0. The host uses this state to write new microcode into the DELUA. In the port halted state, the DELUA does not transmit or receive any frames on the network including maintenance frames. The DELUA responds to port commands, but the only way to get the DELUA out of the port halted state is with the UNIBUS initialization signal, the RESET bit in PCSR0, or by starting the DELUA at an appropriate microcode routine with the start microaddress ancillary function code 1.
UNIBUS Halted	The DELUA enters the UNIBUS halted state when it detects a fatal error in its internal DMA system. When in the UNIBUS halted state, the DELUA also performs the following functions. • Responds to the RESET bit in PCSR0 • Loops frames when requested by another node • Sends system ID frame The DELUA only responds to the UNIBUS initialization signal or the RESET bit in PCSR0.
NI Halted	The DELUA enters the network interconnect (NI) halted state when it detects a fatal error in its internal LANCE system. The DELUA accepts port commands. It also responds to the UNIBUS initialization signal or the RESET bit in PCSR0.
NI and UNIBUS Halted	The DELUA enters the NI and UNIBUS halted state when it detects a fatal internal error. The DELUA only responds to the UNIBUS initialization signal or the RESET bit in PCSR0.

Table 3-2 provides a summary of the events that cause the DELUA to make a transition from one functional state to another.

Table 3-2 Functional State Transition Summary

From State	Transition Event	To State
Any State	Powerup	Reset
	RESET bit in PCSR0 set	Reset
	UNIBUS initialization	Reset
Reset	Selftest ran successfully	Ready
	Selftest already ran successfully	Ready
	Selftest failure – LANCE system	NI Halted
	Selftest failure – DMA system	UNIBUS Halted
	Selftest failure – any other type of internal failure	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset

Table 3-2 Functional State Transition Summary (Cont)

From State	Transition Event	To State
Primary Load	Received memory load with transfer address frame	Secondary Load
	Fatal UNIBUS error	UNIBUS Halted
	Fatal internal error	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
Ready	Port driver START command	Running
	Port driver BOOT command	Primary Load
	Boot frame (with remote boot switch enabled)	Primary Load
	Fatal UNIBUS error	UNIBUS Halted
	Fatal internal error	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
	Port driver HALT command	Port Halted
Running	Port driver STOP command	Ready
	Boot frame (with remote boot switch enabled)	Primary Load
	Fatal UNIBUS error	UNIBUS Halted
	Fatal internal error	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
	Port driver HALT command	Port Halted
Port Halted	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
	Start microaddress ancillary function code 1	State entered depends on microaddress
	Fatal UNIBUS error	UNIBUS Halted
	Fatal internal error	NI and UNIBUS Halted
UNIBUS Halted	Fatal internal error	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
NI Halted	Fatal UNIBUS error	NI and UNIBUS Halted
	Fatal internal error	NI and UNIBUS Halted
	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset
NI and UNIBUS Halted	UNIBUS initialization signal	Reset
	RESET bit in PCSR0 set	Reset

Table 3-3 provides a summary of the state of the internal information retained or reset by the DELUA when making a transition from one state to another.

Table 3-3 State Information Retention Summary

State Entered	State Changes
Reset	Resets the following: Ring formats Counters Physical address Multicast address list Status register Ring pointers Internal memory Load server address System ID PCSRs Mode register
Primary Load State	State information retained depends on the action of the down-line loaded software.
Ready	Retains the following: Ring formats Counters Physical address Multicast address list Mode register Status register Internal memory Load server address System ID PCSRs
Running	Retains everything, resets nothing.
Port Halted	Retains the following: Ring formats Counters Physical address Multicast address list Mode register Status register Internal memory Load server address System ID PCSRs
UNIBUS Halted	Immaterial because you cannot read any status with the UNIBUS halted. All ways of clearing the UNIBUS halted state involve the reset state.
NI Halted	DELUA only enters the NI halted state after executing selftest. All status is cleared at this time.

3.6 POWERUP AND RESET

When the DELUA is turned on, it executes its built-in selftest diagnostic. If the DELUA passes the test, it enters the ready state. If it fails the test, it enters the UNIBUS halted, NI halted, or NI and UNIBUS halted state. It displays the failing error code with the LEDs on the edge of the module (see Table 6-1) and also attempts to report the error code in PCSR1.

The DELUA performs a reset operation when the host sets the reset bit in PCSR0 or when it detects the UNIBUS initialization signal. The DELUA runs selftest only if it failed selftest the last time it ran. If selftest passed last time, the DELUA just clears its registers and counters and enters the ready state.

The following list describes the status of the DELUA registers after powerup or reset.

1. The DELUA physical address equals the default physical address assigned during manufacturing.

2. The multicast address list is empty.

3. The lengths of both the transmit and receive descriptor rings are zero, indicating that the ring specification is invalid.

4. The mode register is clear.

5. The counters are zeros.

6. The DELUA responds to port commands.

7. The DELUA forwards loopback frames to another node.

8. The DELUA sends its system ID frame.

9. The DELUA accepts a remote boot frame from another node.

To set up the DELUA to receive and transmit frames on the network, the the host must perform the following steps.

1. The host enables interrupts by setting the interrupt enable bit in PCSR0.

2. The host writes the base address of the port control block (PCB) into PCSR2 and PCSR3. The PCB is used as an extra set of registers in host memory for issuing ancillary functions to the DELUA.

3. The host writes a GET PCBB port command into PCSR0. This causes the DELUA to read the base address of the PCB from PCSR2 and PCSR3. The DELUA then sets the done interrupt in PCSR0.

4. The host clears the interrupt by writing the done interrupt bit in PCSR0 with a one.

5. The host writes a write descriptor ring format ancillary function code into the PCB. The host also writes the base address of a structure called the UNIBUS data block (UDB) into the PCB.

6. The host writes descriptor ring information into the UDB. This information includes the base addresses and the number of entries in the transmit and receive descriptor rings.

7. The host writes a GET COMMAND port command into PCSR0. This causes the DELUA to read the write descriptor ring format ancillary function from the PCB and store the appropriate descriptor ring information internally. The DELUA then sets the done interrupt in PCSR0.

8. The host clears the interrupt by writing the done interrupt bit in PCSR0 with a one.

9. The host assigns a number of receive data buffers for use by the DELUA by writing the associated entries in the receive descriptor ring. In each entry, the host writes the base address and length of the receive data buffer and sets the ownership bit.

10. The host writes a START port command into PCSR0. This causes the DELUA to change from the ready state to the running state. The DELUA now receives frames addressed to it. The DELUA also transmits message frames when the host issues a POLLING DEMAND port command in PCSR0. The DELUA sets the done interrupt in PCSR0 to acknowledge the START port command.

11. The host clears the interrupt by writing the done interrupt bit in PCSR0 with a one.

3.7 STOP AND RESTART

The host can stop the DELUA from transmitting and receiving frames by writing the STOP port command into PCSR0. This causes the DELUA to change from the running state to the ready state. If the DELUA is transmitting a frame on the network when it receives the STOP command, it finishes transmitting the frame. Otherwise, the DELUA does not transmit or receive any frames except system ID, boot, and loopback MOP frames.

The host can restart the DELUA after a stop by writing the START port command into PCSR0. This causes the DELUA to change from the ready state to the running state. The following parameters remain unchanged by a stop and restart operation.

1. Ring formats
2. Physical address
3. Multicast address list
4. Mode register
5. Status register
6. System ID parameters
7. Internal memory microcode
8. PCSRs

3.8 ANCILLARY FUNCTIONS THAT INTERFERE WITH MESSAGE PROCESSING

Some ancillary functions affect the processing of messages by the DELUA. Table 3-4 shows which functions affect message throughput.

Table 3-4 Ancillary Functions that Interfere with Message Processing

Impact	Function Code	Function Description
None*	0	No Operation
Port†	1	Load and Start Microaddress
None	2	Read Default Physical Address
None	3	No Operation
None	4	Read Physical Address
LANCE‡	5	Write Physical Address
None	6	Read Multicast Address List
LANCE	7	Write Multicast Address List
None	10	Read Ring Format
PORT	11	Write Ring Format
None	12	Read Counters
None	13	Read and Clear Counters
None	14	Read Mode
LANCE	15	Write Mode
None	16	Read Port Status
None	17	Clear Port Status
None	20	Dump Internal Memory
Port	21	Load Internal Memory
None	22	Read Load Server Address
None	23	Write Load Server Address
None	24	Read System ID Parameters
None	25	Write System ID Parameters

Explanation of **Impact** terms:

* None — There is no disturbance to the receive or transmit frame throughput.

† Port — The DELUA does NOT execute these ancillary functions while it is in the running state. These functions execute as a NO-OP. The STOP PORT command must be issued before any of these ancillary functions can be executed.

‡ LANCE — Response to these ancillary functions require the DELUA to temporarily disengage from the network while the mode of the LANCE chip is being modified. The use of these commands can affect the data throughput of the DELUA. Unless it is absolutely necessary, frequent use of these commands is not recommended.

- Reception – The DELUA ignores all frames while modifying LANCE parameters. Frames that the LANCE has already processed and are in the internal memory buffers of the DELUA are sent to the host memory in the normal manner.
- Transmission – The DELUA finishes transmitting the current frame before modifying LANCE parameters.

3.9 SUMMARY OF COMMANDS

Tables 3-5, 3-6, and 3-7 summarize the DELUA commands and functions.

Table 3-5 DELUA Port Commands

Command	Description	Reference Section
STOP	The DELUA stops transmitting and receiving frames.	4.1
START	The DELUA starts transmitting and receiving frames.	4.1
GET PORT CONTROL BLOCK BASE ADDRESS	The DELUA reads the port control block (PCB) base address from the host.	4.1
EXECUTE ANCILLARY FUNCTION	The DELUA reads the ancillary function from the PCB and executes it.	4.1
POLLING DEMAND	The DELUA reads frames from host memory and transmits them on the network.	4.1
BOOT	The DELUA loads its PDP-11 host operating system.	4.1
SELFTEST	The DELUA runs its built-in selftest diagnostic.	4.1
HALT	The DELUA stops all operations and waits for the host to down-line load special microcode.	4.1

Table 3-6 DELUA Ancillary Functions

Function	Description	Reference Section
Read Default Physical Address	Provides the host with the Ethernet physical address of the DELUA.	4.5.3
Read/Write Physical Address	Allows the host to read or change the physical address currently being used by the DELUA.	4.5.5
Read/Write Multicast Address Table	Allows the host to read or write the multicast address table currently being used by the DELUA.	4.5.6
Read/Write Descriptor Ring Format	Allows the host to read or write the current base address and lengths of the transmit and receive descriptor rings.	4.5.7
Read/Write Mode	Allows the host to read or set certain operating features of the DELUA that are used primarily for diagnostic testing.	4.5.9

Table 3-6 DELUA Ancillary Functions (Cont)

Function	Description	Reference Section
Read/Read and Clear Counters	Allows the host to read and clear the error and status counters.	4.5.8
Read/Read and Clear Status	Provides the host with extended status information.	4.5.10
Dump/Load Internal Memory	Allows the host to read and modify the DELUA microcode.	4.5.11
Start Microaddress	Allows the host to start execution of the DELUA microcode at a specified address.	4.5.2
Write System ID Parameters	Allows the host to specify certain parameters that the DELUA sends in its system ID message.	4.5.12
Write Load Server Address	Specifies the preferred node from which the DELUA should get the operating system, when it is booting its PDP-11 host operating system.	4.5.13

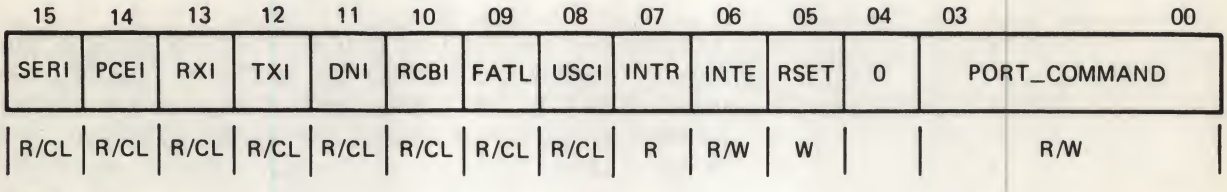
Table 3-7 DELUA Maintenance Functions

Function	Description	Reference Section
Selftest	The DELUA executes its built-in diagnostic test when it receives the SELFTEST port command in PCSR0.	4.1
Loop	The DELUA loops a frame on the network when it receives a loopback frame from another node.	5.5
Identification	The DELUA sends a system ID frame on the network when requested by another node. It also automatically sends a system ID frame about every ten minutes.	5.9
Boot	The DELUA boots its PDP-11 host processor.	5.1

CHAPTER 4
REGISTERS AND COMMANDS

4.1 PORT CONTROL AND STATUS REGISTER 0 (PCSR0)

Figure 4-1 shows the bit format of the PCSR0, and Table 4-1 describes the bit functions.



NOTE:
R/CL = Read Access/ Write one to clear
R = Read Only
RW = Read/Write
W=Write Only

MKV85-1842

Figure 4-1 Port Control and Status Register 0 (PCSR0) Bit Format

Table 4-1 Port Control and Status Register 0 (PCSR0) Bit Descriptions

Bit	Name	Description
⟨15⟩	SERI	Status Error Interrupt – Indicates that there is an error bit set in the DELUA extended status in bits ⟨15:08⟩ of word PCBB+2. Read this status information with the read and clear status, ancillary function codes 16/17. Interrupts the host. Cleared by writing with a one.
⟨14⟩	PCEI	Port Command Error Interrupt – Indicates a function error or a UNIBUS timeout during the execution of a port command. PCSR1 ⟨07⟩ distinguishes between the two error conditions. Interrupts the host. Cleared by writing with a one.
⟨13⟩	RXI	Receive Interrupt – Indicates that the DELUA has placed a frame in a receive data buffer in host memory. Interrupts the host. Cleared by writing with a one.
⟨12⟩	TXI	Transmit Interrupt – Indicates that the DELUA has finished transmitting all the frames on the transmit ring or an error was encountered during a transmission. Interrupts the host. Cleared by writing with a one.
⟨11⟩	DNI	Done Interrupt – Indicates that the DELUA has completed a port command. Interrupts the host. Cleared by writing with a one.

Table 4-1 Port Control and Status Register 0 (PCSR0) Bit Descriptions (Cont)

Bit	Name	Description
⟨10⟩	RCBI	Receive Buffer Unavailable Interrupt – Indicates that the DELUA has discarded an incoming frame because receive buffers were unavailable. This condition occurs when: 1. The DELUA does not own any more data buffers in host memory. The DELUA increments the receive frames lost – local buffer error counter in word UDBB+32 of the extended status information. The host can read this extended status information with the read and clear counters, ancillary function codes 12/13. 2. The DELUA has not been able to write receive data frames into host memory quickly enough and has run out of internal data buffers. The DELUA increments the receive frames lost – internal buffer error counter in word UDBB+30 of the extended status information. The host can read this extended status information with the read and clear counters, ancillary function codes 12/13. Interrupts the host. Cleared by writing with a one. When receive data buffers are available again, the host must issue a POLLING DEMAND port command.
⟨09⟩	FATL	Fatal Internal Error – Indicates that the DELUA has detected a fatal internal error. The status information in PCSR1 is invalid. Interrupts the host. Cleared by writing with a one. The host can attempt to clear the error condition by setting the reset bit ⟨05⟩.
⟨08⟩	USCI	Unsolicited State Change Interrupt – Interrupts when the following occur in the DELUA: 1. Remote boot started – The DELUA receives a boot frame and enters the primary load state. 2. NI halted state – The DELUA detects an error in its LANCE subsystem and enters the NI halted state. These conditions are distinguished by examining the state field ⟨03:00⟩ of PCSR1. Interrupts the host. Cleared by writing with a one.
⟨07⟩	INTR	Interrupt Summary – The logical OR of bits ⟨15:08⟩. Interrupts the host. Cleared by clearing the appropriate error bit(s).
⟨06⟩	INTE	Interrupt Enable – When clear, the DELUA does not interrupt the host. This bit and the port command field ⟨03:00⟩ cannot be written at the same time; two different instructions must be issued.

Table 4-1 Port Control and Status Register 0 (PCSR0) Bit Descriptions (Cont)

Bit	Name	Description
⟨05⟩	RSET	Reset – When set, initializes the DELUA. Note that reset also clears INTE bit ⟨06⟩.
⟨04⟩	Zero	Zero.
⟨03:00⟩	PORT_COMMAND	The port command field and the interrupt enable bit (INTE) ⟨06⟩ cannot be written at the same time; two different instructions must be issued.
		0 0 0 0 NO-OP — Causes no action. Does not set the DNI bit ⟨11⟩.
		0 0 0 1 GET PCBB — Instructs the DELUA to fetch the base address of the port control block (PCB) from PCSR2 and PCSR3.
		0 0 1 0 GET CMD — Instructs the DELUA to fetch and execute an ancillary function from the port control block (PCB).
		0 0 1 1 SELFTEST — Instructs the DELUA to enter the reset state and execute selftest. Selftest takes about 15 seconds. After executing selftest, the DELUA responds by setting the done interrupt bit ⟨11⟩, the unsolicited state change interrupt bit ⟨08⟩, or the fatal error interrupt bit ⟨09⟩. If selftest passes, the DELUA sets the done interrupt bit ⟨11⟩. If selftest fails, but the failure does not prevent the DELUA from communicating with the host, it sets the unsolicited state change interrupt bit ⟨08⟩. In this case, the failing error code is in PSCR1, and the DELUA responds to port commands. If selftest fails, and the failure prevents the DELUA from communicating with the host, the DELUA sets the fatal error interrupt bit ⟨09⟩. The error code information in PCSR1 is invalid.

Table 4-1 Port Control and Status Register 0 (PCSR0) Bit Descriptions (Cont)

Bit	Name	Description					
		0	1	0	0	START	Causes the DELUA to enter the running state. If the DELUA is already in the running state, it does nothing but set the done interrupt bit ⟨11⟩.
		0	1	0	1	BOOT	Instructs the DELUA to enter the primary load state and boot the host system.
		0	1	1	0	Not Used	Reserved code, NO-OP, sets DNI.
		0	1	1	1	Not Used	Reserved code, NO-OP, sets DNI.
		1	0	0	0	PDMD	Polling Demand – Instructs the DELUA to read the descriptor rings to determine if a free buffer has been placed on the receive ring or if a frame is ready for transmission on the transmit ring.
		1	0	0	1	Not Used	Reserved code, NO-OP, sets DNI.
		1	0	1	0	Not Used	Reserved code, NO-OP, sets DNI.
		1	0	1	1	Not Used	Reserved code, NO-OP, sets DNI.
		1	1	0	0	Not Used	Reserved code, NO-OP, sets DNI.
		1	1	0	1	Not Used	Reserved code, NO-OP, sets DNI.
		1	1	1	0	HALT	Causes the DELUA to enter the port halted state. This is the best state for the host to write new microcode into the DELUA. The DELUA does not transmit or receive any messages including MOP messages. If the DELUA is transmitting a frame when it receives the HALT command, it may transmit only a partial frame. Cleared by setting the RESET bit ⟨05⟩, by the UNIBUS initialization signal, or by starting the microcode at an appropriate address with the start microaddress, ancillary function code 1.

Table 4-1 Port Control and Status Register 0 (PCSR0) Bit Descriptions (Cont)

Bit	Name	Description	
		1 1 1 1 STOP	Suspends operation of the DELUA. The DELUA goes from the running state to the ready state. If the DELUA is transmitting a frame, it finishes sending it. If the DELUA is not in the running state, the STOP command acts as a NO-OP and sets the done interrupt (DNI) bit ⟨11⟩.

4.2 PORT CONTROL AND STATUS REGISTER 1 (PCSR1)

PCSR1 is a read-only register. Figure 4-2 illustrates the bit format of PCSR1, and Table 4-2 describes the bit functions.

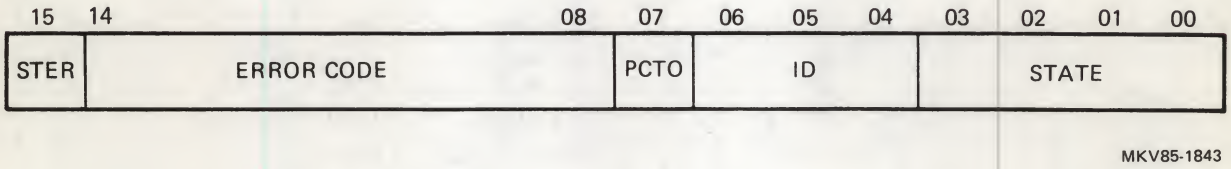


Figure 4-2 Port Control and Status Register 1 (PCSR1) Bit Format

Table 4-2 Port Control and Status Register 1 (PCSR1) Bit Descriptions

Bit(s)	Field	Description
⟨15⟩	STER	Status or Selftest Error – Selftest or the operational microcode has detected an error. Bits ⟨14:08⟩ contain the error code.
⟨14:08⟩	ERROR CODE	Status or Selftest Error Code – The error codes are listed in Table 6-1. Bits ⟨14:08⟩ correspond to LEDs ⟨D3:D9⟩. Note that the DELUA is unable to report errors in this register that involve the DMA system, internal memory, or interrupts.
⟨07⟩	PCTO	Port Command Timeout – Valid only when the port command error interrupt (PCEI) bit ⟨14⟩ of PCSR0 is set. When set, this bit indicates that a UNIBUS timeout occurred while the DELUA was executing a port command. When clear, indicates that the port command contained a function error.
⟨06:04⟩	ID	Identification – Identifies the type of network controller. The DELUA returns 001. The DEUNA returns 000.
⟨03:00⟩	STATE	Table 3-1 describes the functional states.

0	0	0	0	Reset
0	0	0	1	Primary Load
0	0	1	0	Ready
0	0	1	1	Running
0	1	0	0	Not used
0	1	0	1	UNIBUS Halted
0	1	1	0	NI Halted
0	1	1	1	NI and UNIBUS Halted
1	0	0	0	Port Halted
1	0	0	1	Not used (reserved for DELUA)
1	0	1	0	Not used (reserved for DELUA)
1	0	1	1	Not used (reserved for DELUA)
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Secondary Load

4.3 PORT CONTROL AND STATUS REGISTER 2 (PCSR2)

Figure 4-3 illustrates the bit format of PCSR2, and Table 4-3 describes the bit functions.

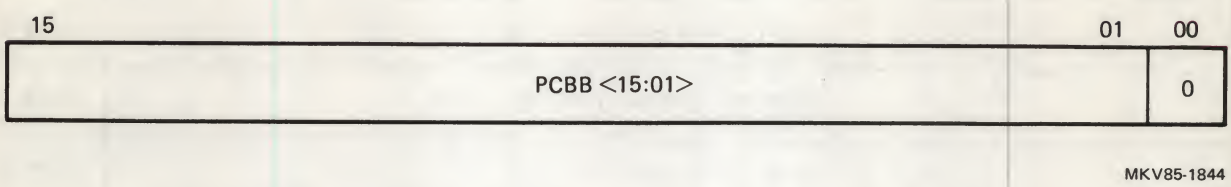


Figure 4-3 Port Control and Status Register 2 (PCSR2) Bit Format

Table 4-3 Port Control and Status Register 2 (PCSR2) Bit Descriptions

Bits	Name	Description
⟨15:01⟩	PCBB	Sixteen low-order address bits of the port control block (PCB) base address.
⟨00⟩	Zero	The PCB base address must be on a word boundary.

4.4 PORT CONTROL AND STATUS REGISTER 3 (PCSR3)

Figure 4-4 illustrates the bit format of PCSR3, and Table 4-4 describes the bit functions.

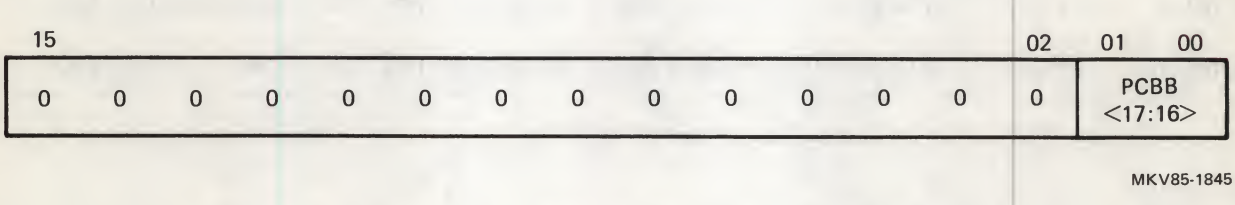


Figure 4-4 Port Control and Status Register 3 (PCSR3) Bit Format

Table 4-4 Port Control and Status Register 3 (PCSR3) Bit Descriptions

Bits	Name	Description
⟨15:02⟩	MBZ	Must be zero.
⟨01:00⟩	PCBB ⟨17:16⟩	Two high-order bits of the port control block (PCB) base address.

4.5 PORT CONTROL BLOCK FUNCTIONS

The port control block (PCB) is four 16-bit words in host memory that the host uses to issue additional commands called ancillary functions to the DELUA. The host tells the DELUA where to find the PCB by issuing the GET PCBB port command. Figure 4-5 shows the PCB bit format, and Table 4-5 describes the bit functions.

PCB

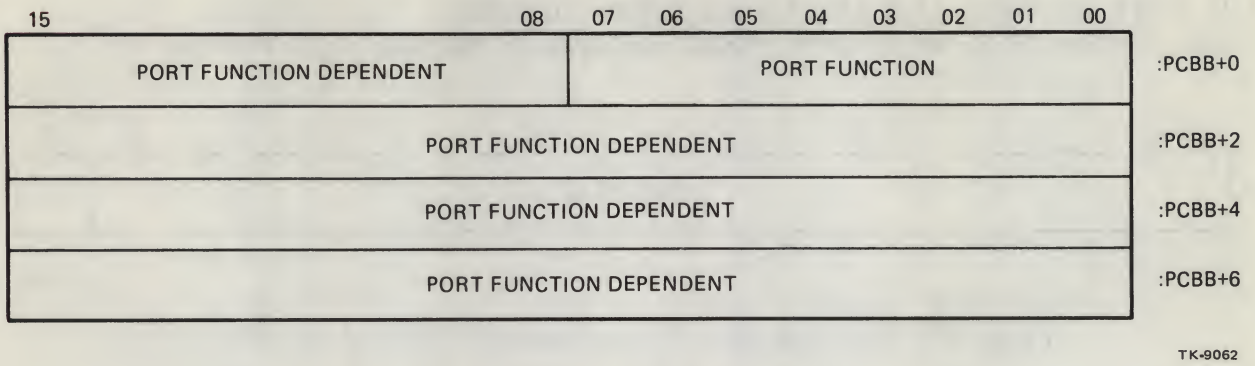


Figure 4-5 Port Control Block (PCB) Bit Format

Table 4-5 Port Control Block (PCB) Bit Descriptions

Word	Bits	Description
PCBB+0	⟨15:08⟩	Interpretation of these bits is dependent upon the PCB ancillary function field ⟨07:00⟩.
PCBB+0	⟨07:00⟩	These bits specify the ancillary function that the DELUA must perform for the port driver. These are written by the port driver and unchanged by the DELUA.
PCBB+2	⟨15:00⟩	Interpretation of these bits is dependent upon the ancillary function field.
PCBB+4	⟨15:00⟩	Interpretation of these bits is dependent upon the ancillary function field.
PCBB+6	⟨15:00⟩	Interpretation of these bits is dependent upon the ancillary function field.

No-Op 0

4.5.1 No-Operation, Ancillary Function Code 0

Figure 4-6 shows the bit format, and Table 4-6 describes the bits for the no-operation function.

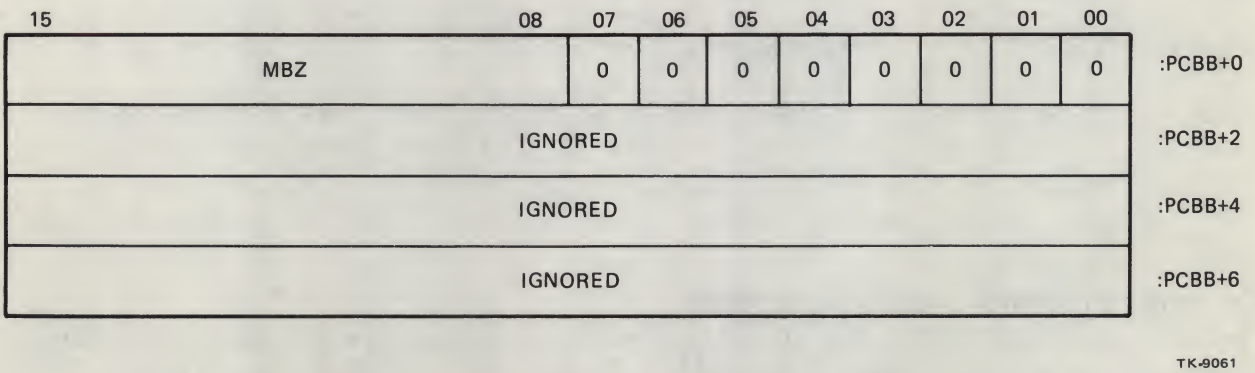


Figure 4-6 No-Operation, Ancillary Function Code 0 Bit Format

Table 4-6 No-Operation, Ancillary Function Code 0 Bit Description

Word	Bits	Field	Description
PCBB+0	⟨07:00⟩	OP CODE	Op code = 0 – NO-OP

4.5.2 Start Microaddress, Ancillary Function Code 1

This function is used by the port driver to instruct the DELUA to start execution of the microcode that the port driver has previously loaded into the DELUA. The port driver loads the microcode with the load internal memory, ancillary function code 21. Figure 4-7 shows the bit format, and Table 4-7 describes the bit functions.

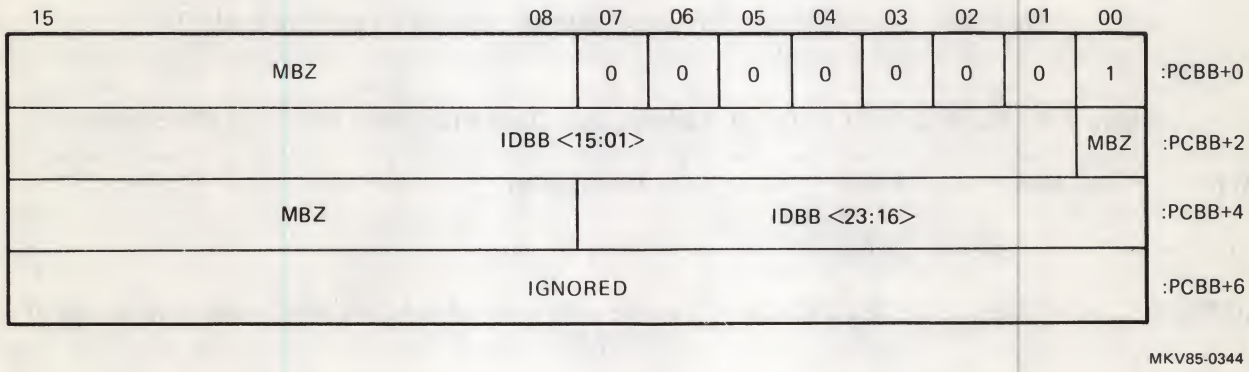


Figure 4-7 Start Microaddress, Ancillary Function Code 1 Bit Format

Table 4-7 Start Microaddress, Ancillary Function Code 1 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 1 – Load and Start Microaddress. Causes the DELUA to start executing from the microaddress supplied in words PCBB+2 and PCBB+4.
PCBB+2	⟨15:01⟩	IDBB ⟨15:01⟩	Bits ⟨15:01⟩ of the internal data block base address from which the DELUA is to start executing.
PCBB+2	⟨00⟩	MBZ	Must be zero. The IDBB must be on a word boundary.
PCBB+4	⟨15:08⟩	MBZ	Must be zero.
PCBB+4	⟨07:00⟩	IDBB ⟨23:16⟩	Bits ⟨23:16⟩ of the internal data block base address from which the DELUA is to start executing.

4.5.3 Read Default Physical Address, Ancillary Function Code 2

This function code allows the host to read the default Ethernet physical address built into the DELUA during manufacturing. Figure 4-8 shows the bit format, and Table 4-8 describes the bit functions.

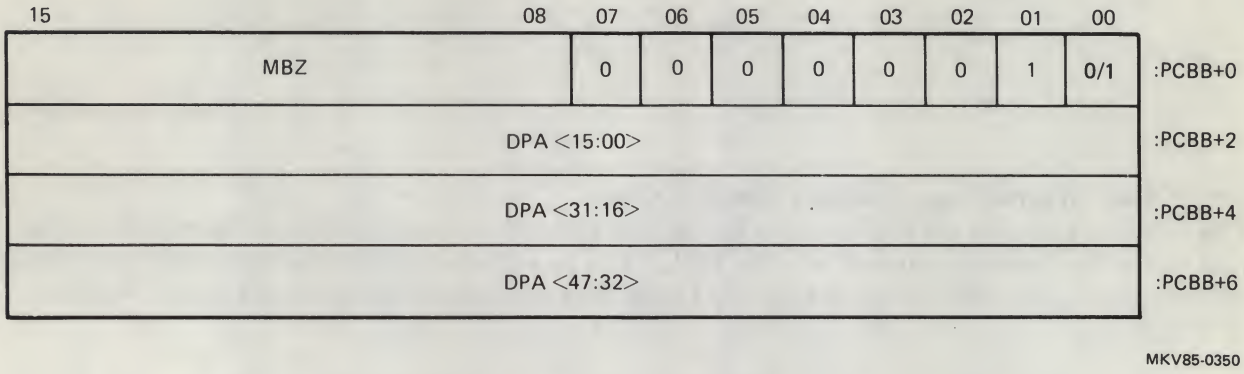


Figure 4-8 Read Default Physical Address, Ancillary Function Code 2 Bit Format

Table 4-8 Read Default Physical Address, Ancillary Function Code 2 Bit Description

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 2 – Read default physical address out of the DELUA.
PCBB+2	⟨15:00⟩	DPA⟨15:00⟩	The low-order 16 address bits of the default physical address.
PCBB+4	⟨15:00⟩	DPA⟨31:16⟩	The middle-order 16 address bits of the default physical address.
PCBB+6	⟨15:00⟩	DPA⟨47:32⟩	The high-order 16 address bits of the default physical address.

4.5.4 No-Operation, Ancillary Function Code 3

This function causes no action in the DELUA.

4.5.5 Read/Write Physical Address, Ancillary Function Codes 4/5

This function allows the port driver to read and write the Ethernet physical address that the DELUA uses for address comparison for incoming frames. Bit ⟨00⟩ of any physical address must always be zero. Figure 4-9 shows the bit format, and Table 4-9 describes the bit functions.

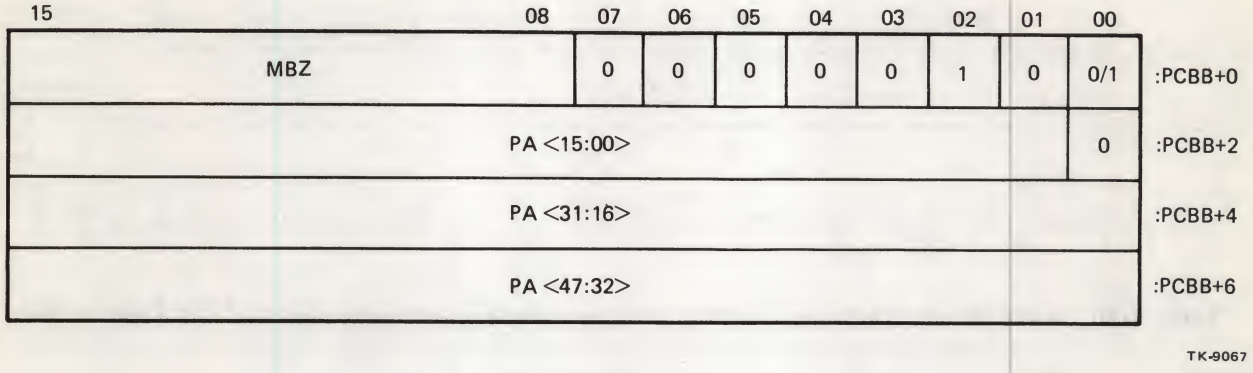


Figure 4-9 Read/Write Physical Address, Ancillary Function Codes 4/5 Bit Format

Table 4-9 Read/Write Physical Address, Ancillary Function Codes 4/5 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 4 – Read the physical address out of the DELUA. Op code = 5 – Write the physical address into the DELUA.
PCBB+2	⟨15:01⟩	PA⟨15:01⟩	Low-order address bits of the physical address.
PCBB+2	⟨00⟩	PA⟨00⟩	Must be zero for physical addresses.
PCBB+4	⟨15:00⟩	PA⟨31:16⟩	Middle-order address bits of the physical address.
PCBB+6	⟨15:00⟩	PA⟨47:32⟩	High-order address bits of the physical address.

4.5.6 Read/Write Multicast Address List, Ancillary Function Codes 6/7

These two function codes enable the port driver to read and write the DELUA multicast address table. A multicast address is an Ethernet address to which a group of logically related stations respond. The DELUA can store up to ten multicast addresses. The read multicast address list ancillary function causes the DELUA to write its current multicast address list into host memory.

Figure 4-10 shows the bit format, and Table 4-10 describes the bit functions. Figure 4-11 shows the bit format of the multicast address list starting at the UDB base address in host memory.

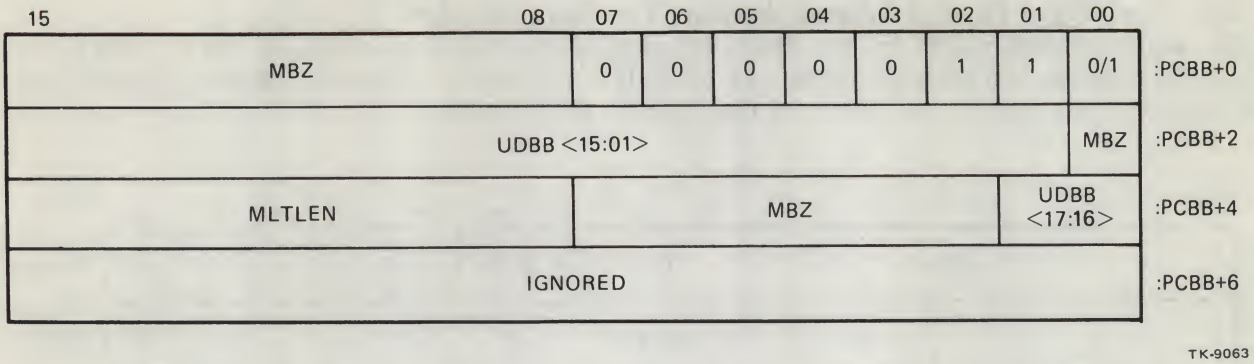


Figure 4-10 Read/Write Multicast Address List, Ancillary Function Codes 6/7 Bit Format

Table 4-10 Read/Write Multicast Address List, Ancillary Function Codes 6/7 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 6 – Read multicast address table out of the DELUA. Op code = 7 – Write multicast address table into the DELUA.
PCBB+2	⟨15:01⟩	UDBB ⟨15:01⟩	UNIBUS data block base address bits ⟨15:01⟩.
PCBB+2	⟨00⟩	MBZ	Bit ⟨00⟩ of the UNIBUS data block base must be zero.
PCBB+4	⟨15:08⟩	MLTLEN	Multicast address table length. The number of multicast addresses to be read or written in the UNIBUS data block. Not more than 10. Since each address takes three words, the length of the UNIBUS data block is three times MLTLEN. Issuing the write multicast address ancillary function with MLTLEN equal to 0 clears the multicast addresses. If the host issues a read multicast address ancillary function with MLTLEN less than the number of multicast addresses in the DELUA, the DELUA returns a truncated list.
PCBB+4	⟨07:02⟩	MBZ	Must be zero.
PCBB+4	⟨01:00⟩	UDBB ⟨17:16⟩	The high-order two address bits of the UNIBUS data block base.

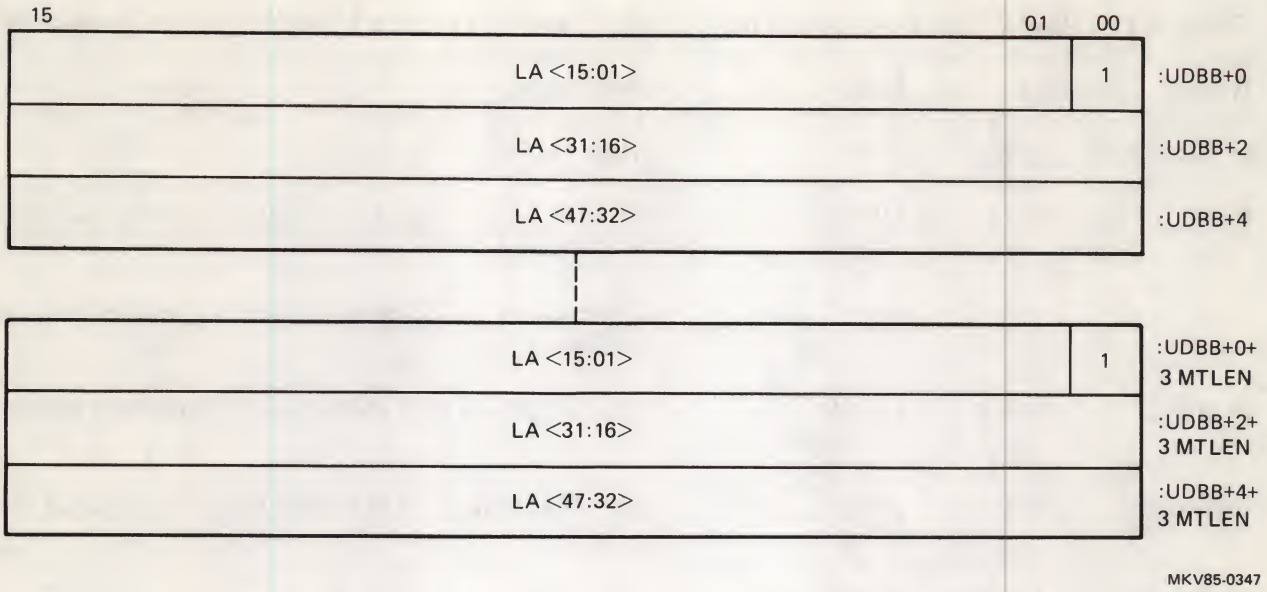


Figure 4-11 Multicast Address List UDB Bit Format

4.5.7 Read/Write Descriptor Ring Format, Ancillary Function Codes 10/11

When initializing the DELUA, the port driver tells the DELUA the size, number, and location of the transmit and receive descriptor ring entries in host memory with the write descriptor ring format function. Issuing the read descriptor ring format function causes the DELUA to write the current value of these parameters into the UDB.

Figure 4-12 shows the bit format, and Table 4-11 describes the bit functions of the read/write descriptor ring format function. Figure 4-13 shows the bit format, and Table 4-12 describes the bit functions of the descriptor ring format information starting at the UDB base address in host memory.

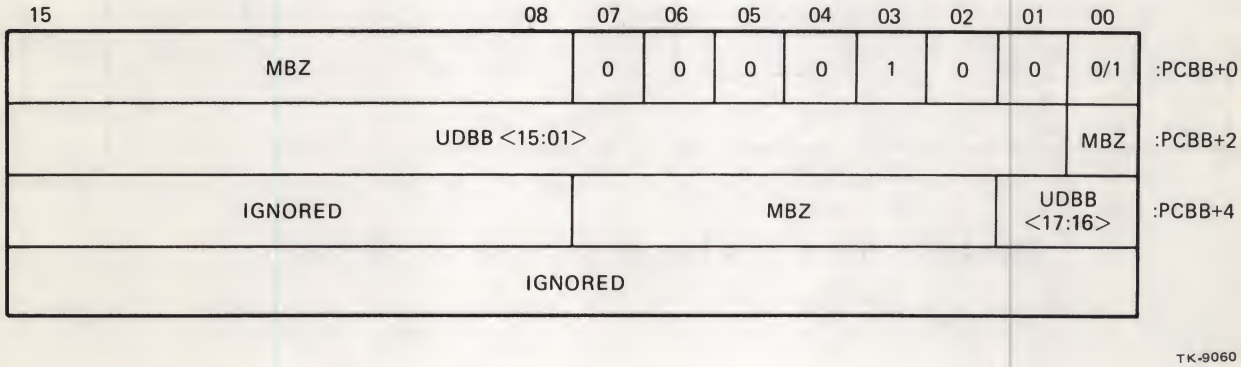


Figure 4-12 Read/Write Descriptor Ring Format, Ancillary Function Codes 10/11 Bit Format

Table 4-11 Read/Write Descriptor Ring Format, Ancillary Function Codes 10/11 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 10 – Read descriptor ring specification out of the DELUA. Op code = 11 – Write descriptor ring specification into the DELUA.
PCBB+2	⟨15:01⟩	UDBB ⟨15:01⟩	Bits ⟨15:01⟩ of the UNIBUS data block base address.
PCBB+2	⟨00⟩	MBZ	Bit ⟨00⟩ of the UNIBUS data block base address must be zero.
PCBB+4	⟨15:08⟩	IGNORED	Not used.
PCBB+4	⟨07:02⟩	MBZ	Must be zero.
PCBB+4	⟨01:00⟩	UDBB ⟨17:16⟩	The high-order two address bits of the UNIBUS data block base.

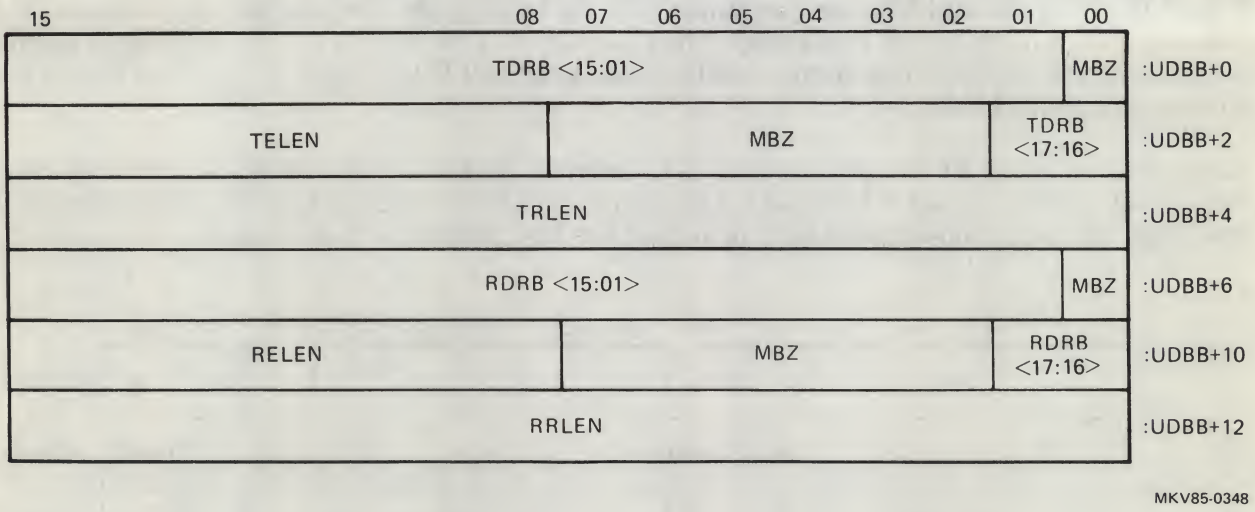


Figure 4-13 Read/Write Descriptor Ring Format UDB Bit Format

Table 4-12 Read/Write Descriptor Ring Format UDB Bit Descriptions

Word	Bits	Field	Description
UDBB+0	⟨15:01⟩	TDRB	Address bits ⟨15:01⟩ of the transmit descriptor ring base.
UDBB+0	⟨00⟩	MBZ	Must be zero.
UDBB+2	⟨15:08⟩	TELEN	Number of words in each entry in the transmit descriptor ring. TELEN must be greater than or equal to 4.
UDBB+2	⟨07:02⟩	MBZ	Must be zero.
UDBB+2	⟨01:00⟩	TDRB ⟨17:16⟩	The high-order two address bits of the transmit descriptor ring base address.
UDBB+4	⟨15:00⟩	TRLEN	Number of entries in the transmit descriptor ring.
UDBB+6	⟨15:01⟩	RDRB	Address bits ⟨15:01⟩ of the receive descriptor ring base address.
UDBB+6	⟨00⟩	MBZ	Must be zero.
UDBB+10	⟨15:08⟩	RELEN	Number of words in each entry in the transmit descriptor ring. RELEN must be greater than or equal to 4.
UDBB+10	⟨07:02⟩	MBZ	Must be zero.
UDBB+10	⟨01:00⟩	RDRB ⟨17:16⟩	The high-order two address bits of the receive descriptor ring base.
UDBB+12	⟨15:00⟩	RRLEN	Number of entries in the receive descriptor ring. Must be 2 or more.

4.5.8 Read/Read and Clear Counters, Ancillary Function Codes 12/13

The Read Counters function is used by the port driver to read the counters held by the DELUA. The read and clear counters function sets the counters to zero after reading them. Figure 4-14 shows the bit format, and Table 4-13 describes the bit functions.

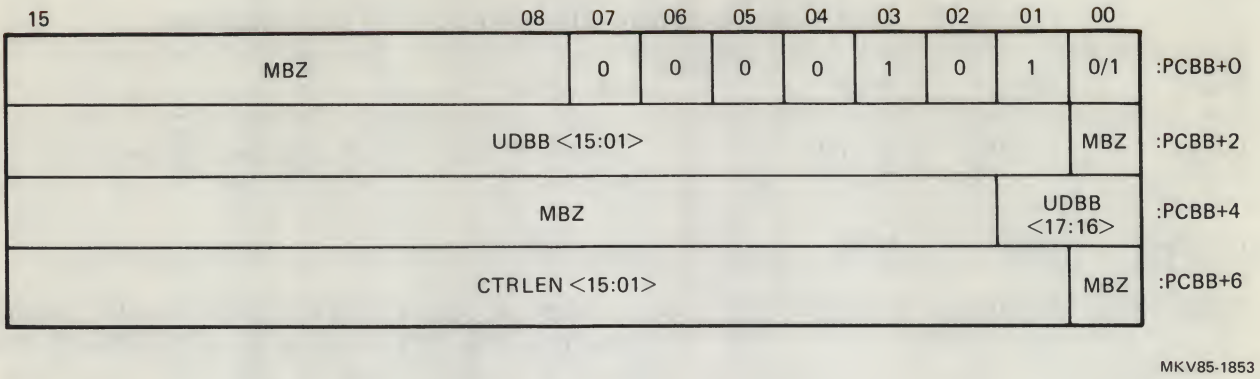


Figure 4-14 Read/Read and Clear Counters, Ancillary Function Codes 12/13 Bit Format

Table 4-13 Read/Read and Clear Counters, Ancillary Function Codes 12/13 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 12 – Read counters out of the DELUA. Op code = 13 – Read counters out of the DELUA and clear counters.
PCBB+2	⟨15:01⟩	UDBB	Bits ⟨15:01⟩ of the UNIBUS data block base. These are written by the port driver and unchanged by the DELUA.
PCBB+2	⟨00⟩	MBZ	Bit ⟨00⟩ of the UNIBUS data block base. Must be zero.
PCBB+4	⟨15:02⟩	MBZ	Must be zero.
PCBB+4	⟨01:00⟩	UDBB	The high-order address bits ⟨17:16⟩ of the UNIBUS data block base.
PCBB+6	⟨15:01⟩	CTRLEN	Counter List Length – Length of the UNIBUS data block in words, up to 55 decimal. With a length of less than 55, the DELUA returns a truncated list.
PCBB+6	⟨00⟩	MBZ	Must be zero.

Counter values are unsigned integers. Counters latch at their maximum values to indicate overflow. Figure 4-15 shows the bit format, and Table 4-14 describes the bit functions of the counter list starting at the UDB base address in host memory.

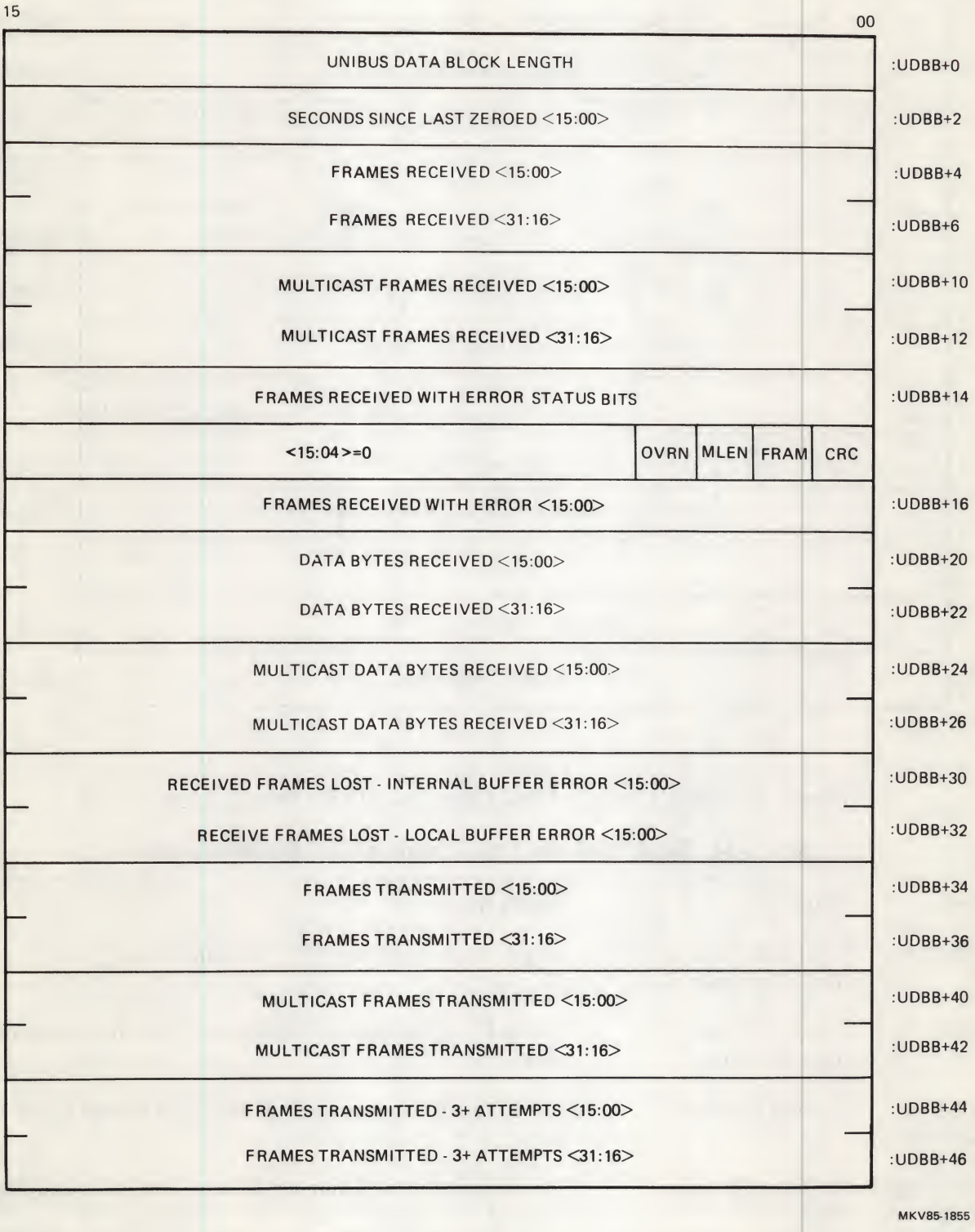


Figure 4-15 Read/Read and Clear Counters UDB Bit Format (Sheet 1 of 2)

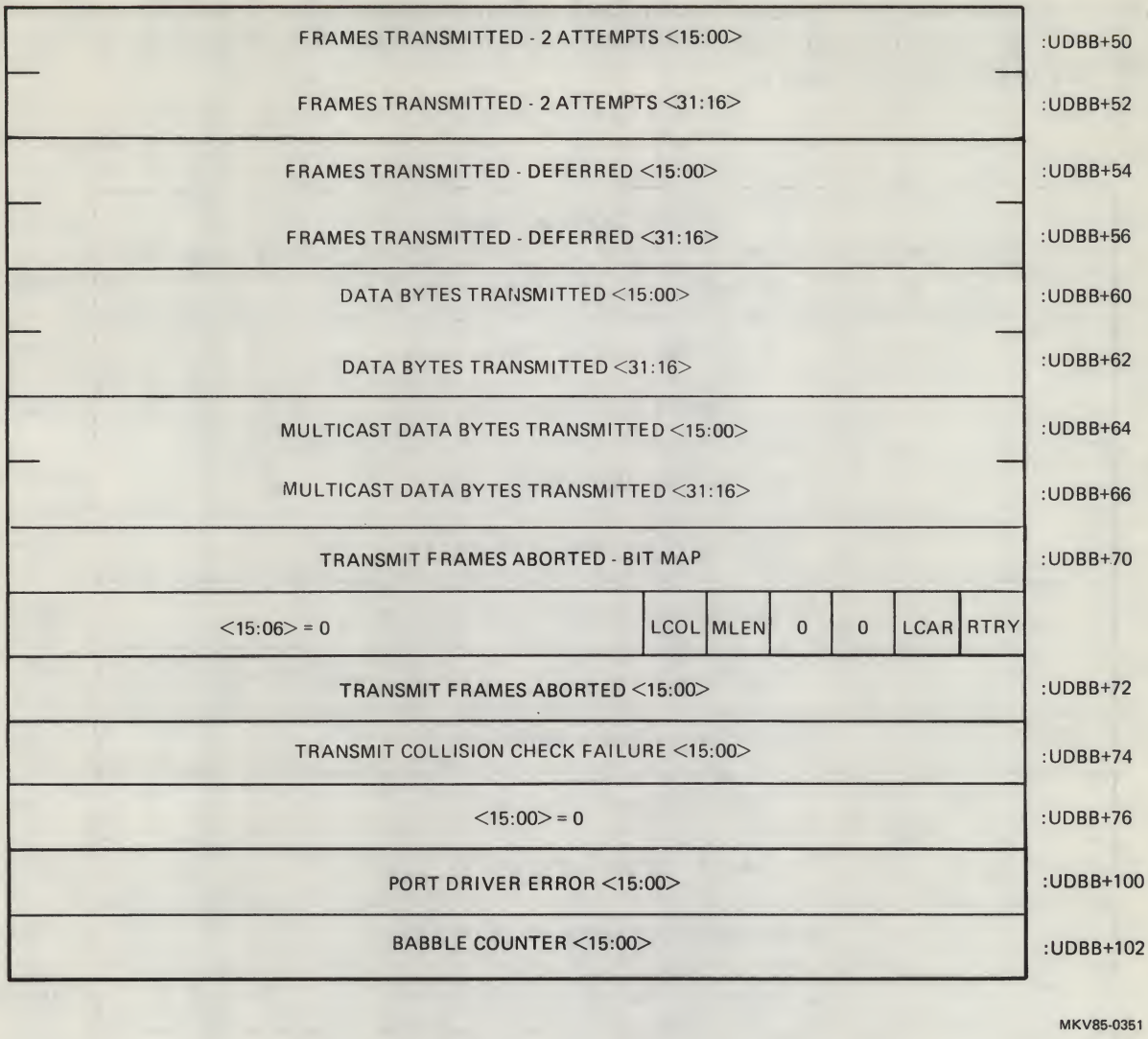


Figure 4-15 Read/Read and Clear Counters UDB Bit Format (Sheet 2 of 2)

Table 4-14 Read/Read and Clear Counters UDB Bit Descriptions

Word	Name	Description
UDBB+0	UNIBUS Data Block Length	Length in words of the UNIBUS data block.
UDBB+2	Seconds Since Last Zeroed	16 bits for the number of seconds since the counters were last zeroed.
UDBB+4 UDBB+6	Frames Received	32 bits for the total number of error-free frames received.
UDBB+10 UDBB+12	Multicast Frames Received	32 bits for the total number of error-free multicast frames received.

Table 4-14 Read/Read and Clear Counters UDB Bit Descriptions (Cont)

Word	Name	Description
UDBB+14	Frames Received with Error Status Bits	Indicates the types of receive errors that have occurred since the last time the counters were cleared.

Status Bits

Bit(s)	Name	Description
⟨15:04⟩		Not used.
⟨03⟩	OVRN	Overrun Error – The DELUA lost part or all of one or more frames because the LANCE system was unable to write the data into internal memory as fast as it received the frame from the network. Overrun error is also reported by OVRN bit ⟨12⟩ of word RDRB+6 in the receive descriptor ring entry.
⟨02⟩	MLEN	Message Length Error – A frame was larger than 1518 bytes.
⟨01⟩	FRAM	Framing Error – A frame did not contain a multiple of 8 bits. Also reported by FRAM bit ⟨13⟩ of word RDRB+4 in the receive descriptor ring entry.
⟨00⟩	CRC	Block Check Error – A frame failed the CRC check. Also reported by CRC bit ⟨11⟩ of word RDRB+4 in the receive descriptor ring entry.

UDBB+16	Frames Received with Error	16 bits for the total number of frames received with one or more errors.
UDBB+20 UDBB+22	Data Bytes Received	32 bits for the total number of data bytes received error-free.
UDBB+24 UDBB+26	Multicast Bytes Received	32 bits for the total number of error-free multicast data bytes received.
UDBB+30	Receive Frame Lost – Internal Buffer Error	16 bits for the total number of times there was a discard of an incoming frame due to lack of internal buffer space. Incoming frames must be error-free to be counted.

Table 4-14 Read/Read and Clear Counters UDB Bit Descriptions (Cont)

Word	Name	Description
UDBB+32	Receive Frames Lost – Local Buffer Error	16 bits for the total number of times there was a problem with a receive ring data buffer. This counter is incremented on one or more of the following occurrences: • Buffer unavailable – A frame was lost because there was no available buffer on the receive ring. • Buffer too small – A frame was truncated because it was larger than the available buffer space on the receive ring.
UDBB+34 UDBB+36	Frames Transmitted	32 bits for the total number of frames successfully transmitted, including transmissions in which the collision test signal failed to assert.
UDBB+40 UDBB+42	Multicast Frames Transmitted	32 bits for the total number of multicast frames successfully transmitted, including transmissions in which the collision test signal failed to assert.
UDBB+44 UDBB+46	Frames Transmitted 3+ Attempts	32 bits for the total number of frames successfully transmitted on three or more attempts, including transmissions in which the collision test signal failed to assert.
UDBB+50 UDBB+52	Frames Transmitted 2 Attempts	32 bits for the total number of frames successfully transmitted on two attempts, including transmissions in which the collision test signal failed to assert.
UDBB+54 UDBB+56	Frames Transmitted Deferred	32 bits for the total number of frames successfully transmitted on the first attempt after deferring, including transmissions in which the collision test signal failed to assert.
UDBB+60 UDBB+62	Data Bytes Transmitted	32 bits for the total number of data bytes successfully transmitted, including transmissions in which the collision test signal failed to assert.
UDBB+64 UDBB+66	Multicast Bytes Transmitted	32 bits for the total number of multicast data bytes successfully transmitted, including transmissions in which the collision test signal failed to assert.
UDBB+70	Transmit Frames Aborted Status Bits	Indicates the types of transmit errors that have occurred since the last time the counters were cleared. **Status Bits** **Bit(s) Name Description** ⟨15:06⟩ Not Used Zero.

Table 4-14 Read/Read and Clear Counters UDB Bit Descriptions (Cont)

Word	Name	Description		
		⟨05⟩	LCOL	Late collision – A collision occurred after all nodes on the network should have known there was a frame being transmitted. Suggests that the collision detection circuitry of some node may have failed. Also reported in LCOL bit ⟨12⟩ of word TDRB+6 in the transmit descriptor ring entry.
		⟨04⟩	MLEN	Data block too long – The DELUA aborted a transmission because the frame exceeded the maximum frame size.
		⟨03⟩	Not Used	Zero.
		⟨02⟩	Not Used	Zero.
		⟨01⟩	LCAR	Loss of carrier – Carrier went away while transmission was in progress. Also reported in LCAR bit ⟨11⟩ of word TDRB+6 in the transmit descriptor ring entry.
		⟨00⟩	RTRY	Excessive collisions – Retry error, 16 unsuccessful transmission attempts. Also reported in RTRY bit ⟨10⟩ of word TDRB+6 in the transmit descriptor ring entry.
UDBB+72	Transmit Frames Aborted	16 bits for the total number of frames that were aborted during transmission for one or more of the errors reported in UDBB+70.		
UDBB+74	Transmit Collision Check Failure	16 bits for the total number of times the collision test signal failed to assert following an apparently successful transmission. The DELUA occasionally increments this counter when there has not been a collision test signal failure. The number of transmit collision checks that can be expected varies with network message traffic, but one check in 10,000 frames transmitted is typical. If the DELUA logs as many as one check in 100 frames transmitted, a fault in the network transceiver should be suspected. Some network transceivers made by other companies do not have a collision test signal. In this case, you will see one failure for every frame transmitted.		

Table 4-14 Read/Read and Clear Counters UDB Bit Descriptions (Cont)

Word	Name	Description
UDBB+76	Not Used	Zeros.
UDBB+100	Port Driver Error	16 bits for the total number of times the host attempted to issue a port command or ancillary function while one was still being processed.
UDBB+102	Babble Counter	16 bits for the total number of times the LANCE truncated an excessively long frame transmission. The LANCE contains a timer that stops transmission if the transmitter is on for a time longer than the time to transmit a maximum length frame.

Read/Write Mode Register 14/15

4.5.9 Read/Write Mode Register, Ancillary Function Codes 14/15

This ancillary function is used by the port driver to read or write the DELUA mode register. The mode register is used to program the operation of the DELUA while the DELUA is in the running state. Figure 4-16 shows the bit format, and Table 4-15 describes the bit functions.

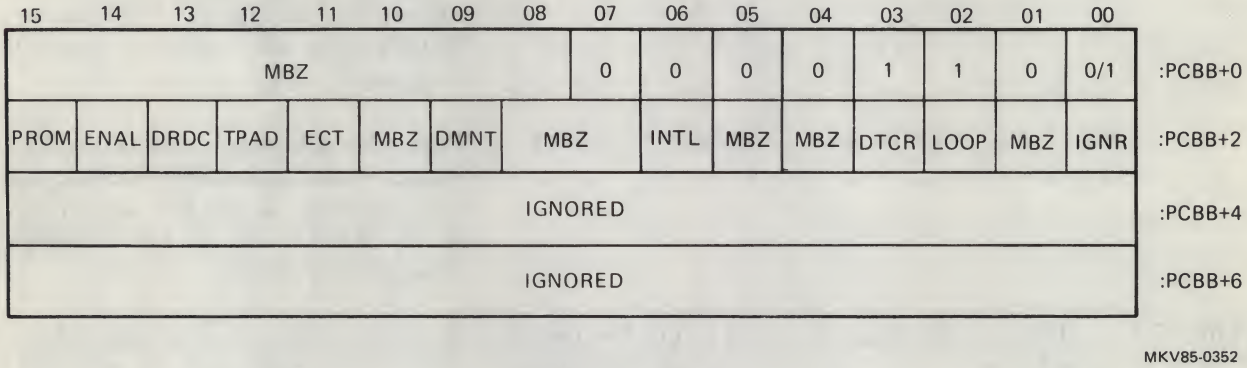


Figure 4-16 Read/Write Mode Register, Ancillary Function Codes 14/15 Bit Format

Table 4-15 Read/Write Mode Register, Ancillary Function Codes 14/15 Bit Descriptions

Word	Bit(s)	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 14 – Read the mode out of the DELUA.
			Op code = 15 – Write the mode into the DELUA.

Table 4-15 Read/Write Mode Register, Ancillary Function Codes 14/15 Bit Descriptions (Cont)

Word	Bit(s)	Field	Description
PCBB+2	⟨15⟩	PROM	Promiscuous Mode – Instructs the DELUA to accept all incoming frames regardless of their destination address field. This bit is clear after powerup.
PCBB+2	⟨14⟩	ENAL	Enable All – Instructs the DELUA to accept all incoming frames with multicast destinations. This bit is clear after powerup.
PCBB+2	⟨13⟩	DRDC	Disable data chaining mode on received frames. When the DELUA is in this mode, it will truncate frames that do not fit in a single buffer. This bit is clear after powerup.
PCBB+2	⟨12⟩	TPAD	Transmit Pad Enable – Causes the DELUA to add zeros to the data field of frames with a data field less than 64 bytes long.
PCBB+2	⟨11⟩	ECT	Enable Collision Test – When set, the collision test error (CERR) bit ⟨12⟩ of word PCBB+2 of the extended status information generates an interrupt to the host. The host can read this extended status information with the read and clear status, ancillary function codes 16/17. This bit is clear after powerup.
PCBB+2	⟨10⟩	MBZ	Must be zero.
PCBB+2	⟨09⟩	DMNT	Disable Maintenance Message – Instructs the DELUA not to transmit a response to, and to discard all incoming loop, boot, and request ID messages. In addition, the DELUA does not issue the system ID message. This is an aid in running on-line diagnostics.
PCBB+2	⟨08:07⟩	MBZ	Must be zero.
PCBB+2	⟨06⟩	INTL	Internal Loopback – Used with the LOOP ⟨02⟩ bit to determine where the loopback is to be done. Internal loopback allows DELUA/LANCE to receive its own transmitted frame. The frame size is limited to the silo size in the LANCE. The number of bytes that can be looped also depends on the state of the DTCR bit in the mode register. See Section 5.5. INTL is only valid if LOOP = 1.

Table 4-15 Read/Write Mode Register, Ancillary Function Codes 14/15 Bit Descriptions (Cont)

Word	Bit(s)	Field	Description
			Loop **Intl** **Loopback** 0 0 Normal operation, no loopback 0 1 Port command error 1 0 External loopback 1 1 Internal loopback This bit is clear after powerup.
PCBB+2	⟨05:04⟩	MBZ	Must be zero.
PCBB+2	⟨03⟩	DTCR	Causes the DELUA to omit the CRC bytes when transmitting frames. Also disables the processing of maintenance messages such as loopback, system ID, and boot messages. This bit is clear after powerup.
PCBB+2	⟨02⟩	LOOP	Causes the DELUA to receive frames that it transmits. The maximum frame size is 32 bytes if DTCR is 0 or 36 bytes if DTCR is a 1. See Section 5.5. Also disables the processing of maintenance messages such as loopback, system ID, and boot messages. This bit is clear after powerup.
PCBB+2	⟨01⟩	MBZ	Must be zero.
PCBB+2	⟨00⟩	IGNORED	This bit is ignored by the DELUA.

Read and Clear Status 16/17

4.5.10 Read/Read and Clear Status, Ancillary Function Codes 16/17

This function is used by the port driver to read and clear status from the DELUA. Function code 17 clears the high byte of PCBB+2. Figure 4-17 shows the bit format, and Table 4-16 describes the bit functions.

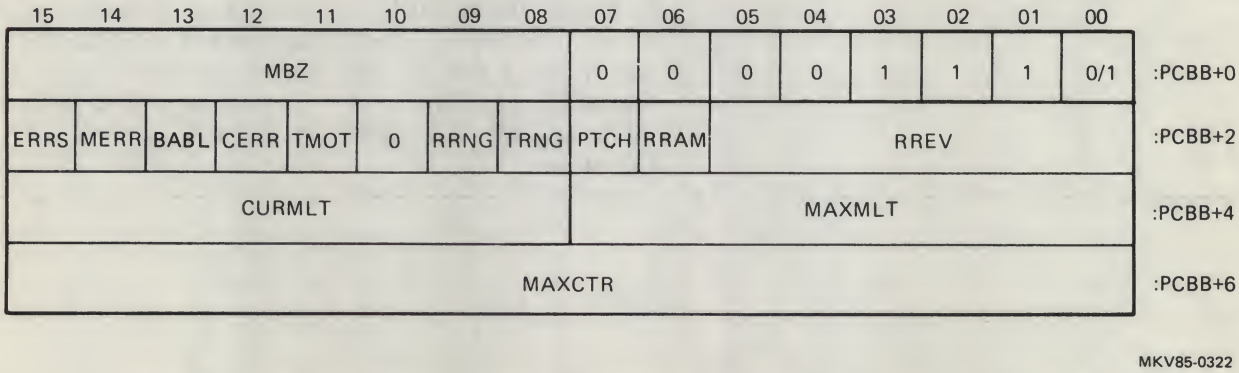


Figure 4-17 Read/Read and Clear Status, Ancillary Function Codes 16/17 Bit Format

Table 4-16 Read/Read and Clear Status, Ancillary Function Codes 16/17 Bit Descriptions

Word	Bit(s)	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 16 – Read status out of the DELUA. Op code = 17 – Read status out of the DELUA and clear status in the DELUA.
PCBB+2	⟨15⟩	ERRS	Error Summary – Logical OR of MERR ⟨14⟩, BABL ⟨13⟩, CERR ⟨12⟩, TMOT ⟨11⟩, RRNG ⟨09⟩, and TRNG ⟨08⟩. Also sets SERI bit ⟨15⟩ in PCSR0, which generates an interrupt.
PCBB+2	⟨14⟩	MERR	Multiple Errors – Indicates that one or more of the following error conditions reoccurred before the host read status with the read and clear status ancillary function: TMOT ⟨11⟩, RRNG ⟨09⟩, or TRNG ⟨08⟩.
PCBB+2	⟨13⟩	BABL	Indicates that the transmitter has been on longer than the time required to send the maximum length frame.
PCBB+2	⟨12⟩	CERR	Collision Test Error – The transceiver failed to send the collision test signal at the end of a transmission. Occasionally the DELUA detects this condition erroneously. See the transmit collision check failure counter in word UDBB+74 of the read and clear counters, ancillary function codes 12/13. This bit is only active when enabled by ECT, bit ⟨11⟩ of word PCBB+2 of the write mode register, ancillary function code 15.
PCBB+2	⟨11⟩	TMOT	Timeout Error – UNIBUS timeout error encountered while performing a ring access. This bit indicates that either a nonexistent UNIBUS address was accessed or the DELUA timed out waiting for a DMA request on the UNIBUS.
PCBB+2	⟨10⟩	MBZ	Must be zero.
PCBB+2	⟨09⟩	RRNG	Receiver Ring Error – The DELUA encountered an error while accessing the receive descriptor ring.
PCBB+2	⟨08⟩	TRNG	Transmit Ring Error – The DELUA encountered an error while accessing the transmit descriptor ring.
PCBB+2	⟨07⟩	PTCH	ROM Patch – When set, indicates that a change or modification has been made to the DELUA operational microcode.

Table 4-16 Read/Read and Clear Status, Ancillary Function Codes 16/17 Bit Descriptions (Cont)

Word	Bit(s)	Field	Description
PCBB+2	⟨06⟩	RRAM	RAM Microcode Operational – The DELUA is executing out of RAM rather than ROM microcode.
PCBB+2	⟨05:00⟩	RREV	ROM Revision – The revision number of the DELUA on-board microcode.
PCBB+4	⟨15:08⟩	CURMLT	The current number of multicast addresses residing in the DELUA; zero upon powerup.
PCBB+4	⟨07:00⟩	MAXMLT	Maximum number of multicast addresses (10) the DELUA will support.
PCBB+6	⟨15:00⟩	MAXCTR	Maximum length in words of the data block reserved for counters (34).

4.5.11 Dump/Load Internal Memory, Ancillary Function Codes 20/21

These functions allow the host to read the contents of DELUA internal memory and to write new microcode into DELUA internal memory. Figure 4-18 shows the bit format, and Table 4-17 describes the bit functions. Figure 4-19 shows the bit format, and Table 4-18 describes the bit functions of the associated parameters starting at the UDB base address in host memory.

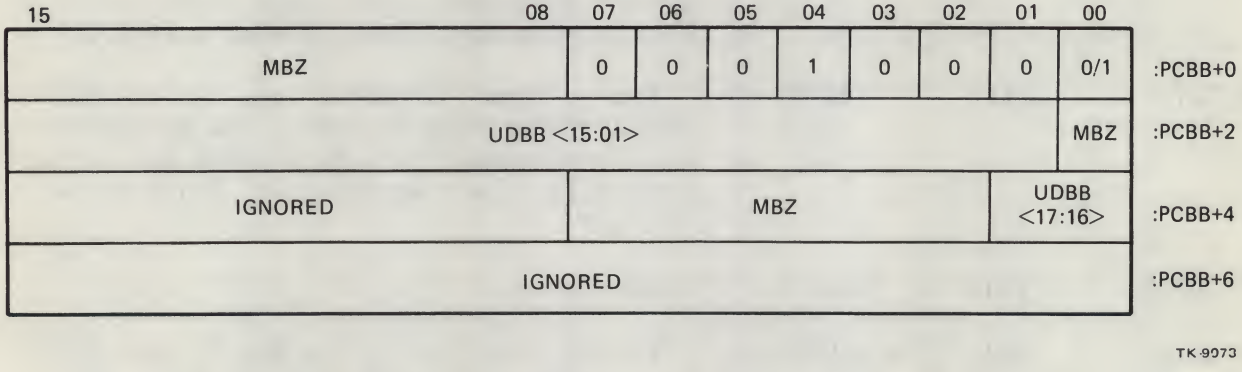


Figure 4-18 Dump/Load Internal Memory, Ancillary Function Codes 20/21 Bit Format

Table 4-17 Dump/Load Internal Memory, Ancillary Function Codes 20/21 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 20 – Dump DELUA internal memory. Op code = 21 – Load DELUA internal memory.
PCBB+2	⟨15:01⟩	UDBB	Address bits ⟨15:01⟩ of the UNIBUS data block base.
PCBB+2	⟨00⟩	MBZ	Must be zero.
PCBB+4	⟨15:08⟩	IGNORED	Ignored by the DELUA.
PCBB+4	⟨07:02⟩	MBZ	Must be zero.
PCBB+4	⟨01:00⟩	UDBB	The high-order address bits ⟨17:16⟩ of the UNIBUS data block base.
PCBB+6	⟨15:00⟩	IGNORED	Ignored by the DELUA.

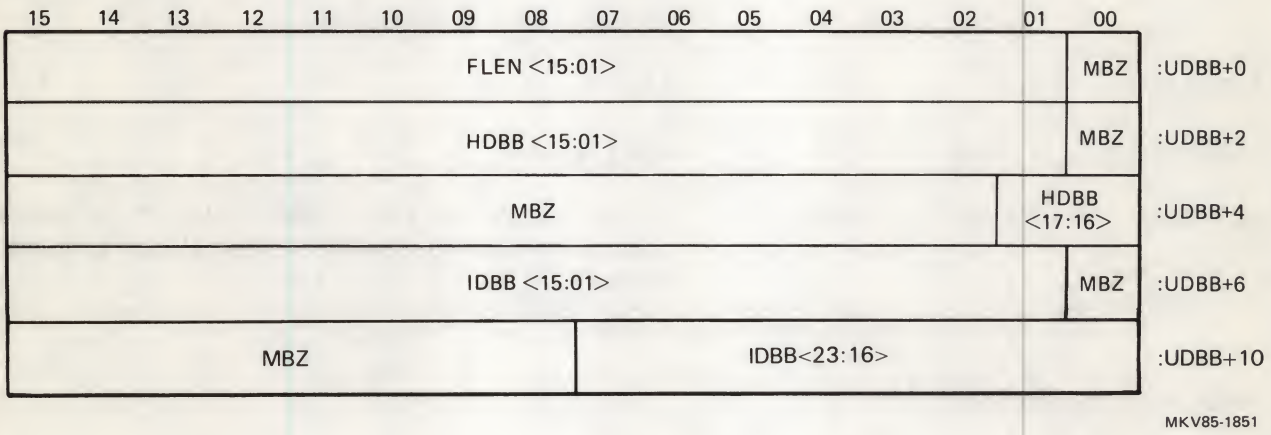


Figure 4-19 Dump/Load Internal Memory UDB Bit Format

Table 4-18 Dump/Load Internal Memory UDB Bit Descriptions

Word	Bits	Field	Description
UDBB+0	⟨15:01⟩	FLEN	Field Length – The number of words to be transferred between host memory and DELUA internal memory.
UDBB+0	⟨00⟩	MBZ	Must be zero.
UDBB+2	⟨15:01⟩	HDBB	Host Data Block Base – Bits ⟨15:01⟩ of the starting address of the data buffer in host memory.
UDBB+2	⟨00⟩	MBZ	Must be zero.
UDBB+4	⟨15:02⟩	MBZ	Must be zero.
UDBB+4	⟨01:00⟩	HDBB	Host Data Block Base – Bits ⟨17:16⟩ of the starting address of the data buffer in host memory.
UDBB+6	⟨15:01⟩	IDBB	Internal Data Block Base – Bits ⟨15:01⟩ of the starting address of the data buffer in the DELUA internal memory. The host can read addresses 0 to 1FFFE and 80000 to 83FFE. When the DELUA is in the port halted state, the host can write addresses 4400 to 1FFFE. When the DELUA is in the ready state, the host can only write addresses 4400 to 6400 hex.
UDBB+6	⟨00⟩	MBZ	Must be zero.
UDBB+10	⟨15:08⟩	MBZ	Must be zero.
UDBB+10	⟨07:00⟩	IDBB	Internal Data Block Base – Bits ⟨23:16⟩ of the starting address of the data buffer in the DELUA internal memory.

4.5.12 Read/Write System ID Parameters, Ancillary Function Codes 22/23

This function allows the host to read or write the parameters that the DELUA sends in the request program and system ID frames and the verification code for boot functions. Figure 4-20 shows the bit format, and Table 4-19 describes the bit functions. Figure 4-21 shows the bit format, and Table 4-20 describes the bit functions of the system ID parameter list that starts at the UDB base address in host memory.

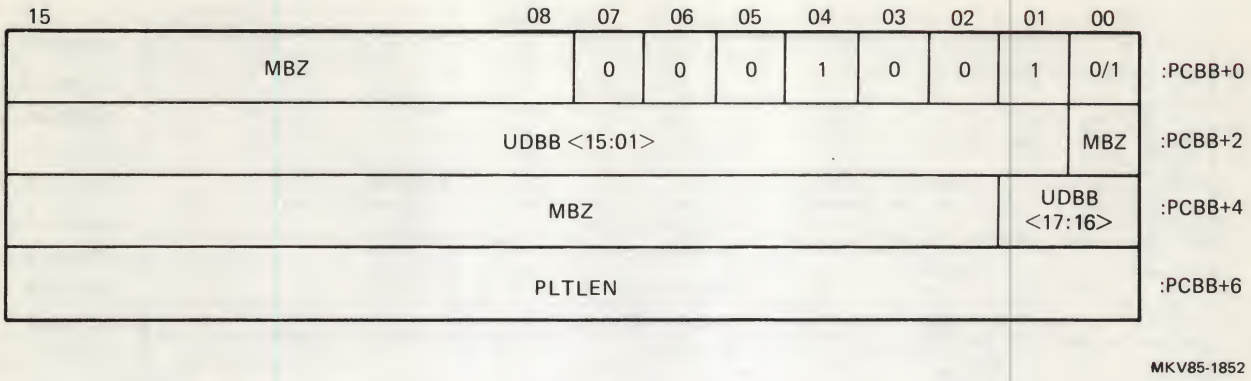


Figure 4-20 Read/Write System ID Parameters, Ancillary Function Codes 22/23 Bit Format

Table 4-19 Read/Write System ID Parameters, Ancillary Function Codes 22/23 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 22 – Read system ID parameter list out of the DELUA. Op code = 23 – Write system ID parameter list into the DELUA.
PCBB+2	⟨15:01⟩	UDBB	The low-order address bits ⟨15:01⟩ of the UNIBUS data block base.
PCBB+2	⟨00⟩	MBZ	Must be zero.
PCBB+4	⟨15:02⟩	MBZ	Must be zero.
PCBB+4	⟨01:00⟩	UDBB	The high-order address bits ⟨17:16⟩ of the UNIBUS data block base.
PCBB+6	⟨15:00⟩	PLTLEN	System ID Parameter List Length – The length in words of the UNIBUS data block. The maximum value of PLTLEN is 100 decimal. When reading the system ID parameter list and the PLTLEN field is less than 100 (decimal) words, the DELUA returns, without error, a truncated list equal to the number asked for, starting with the first entry in the list. When reading or writing the system ID parameter list and the PLTLEN field is greater than 100 (decimal) words, the DELUA aborts the command and sets the appropriate error status.

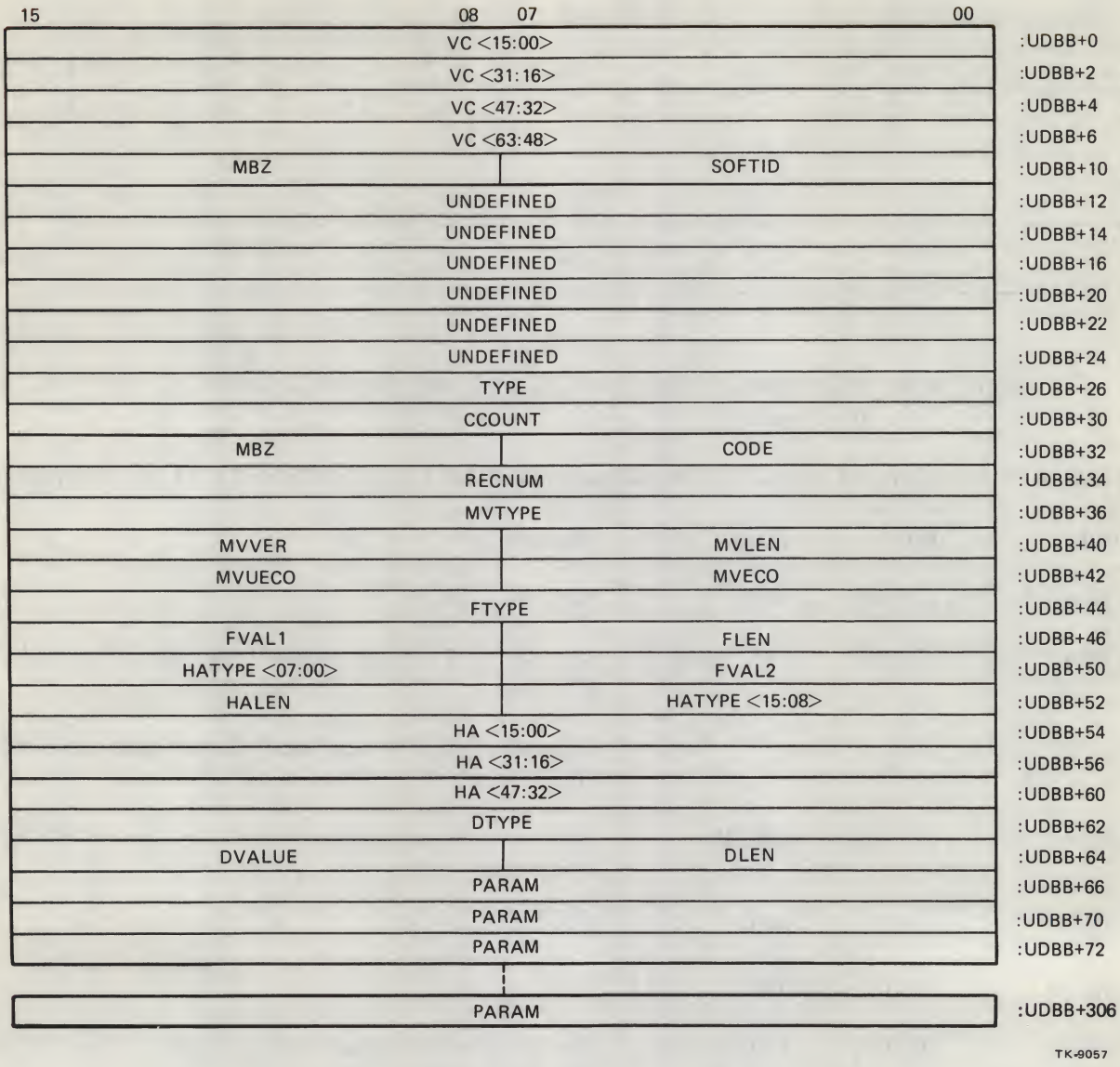


Figure 4-21 Read/Write System ID Parameters UDB Bit Format

Table 4-20 Read/Write System ID Parameters UDB Bit Format

Word	Bits	Field	Description
UDBB+0	⟨15:00⟩	VC⟨15:00⟩	Word 0 of the boot verification code.
UDBB+2	⟨15:00⟩	VC⟨31:16⟩	Word 1 of the boot verification code.
UDBB+4	⟨15:00⟩	VC⟨47:32⟩	Word 2 of the boot verification code.
UDBB+6	⟨15:00⟩	VC⟨63:48⟩	Word 3 of the boot verification code. When the DELUA receives a boot frame, it checks the verification code in the boot frame against this verification code. If the codes do not match, the DELUA ignores the boot frame. If this code is zero, the DELUA accepts any verification code. The default value is zero.
UDBB+10	⟨15:08⟩	MBZ	Must be zero.
UDBB+10	⟨07:00⟩	SOFTID	Software Identification – Specifies the type of software the DELUA asks for in a request program frame in response to a BOOT port command in PCSR0. The default value is zero.
UDBB+12	⟨15:00⟩	Undefined	
UDBB+14	⟨15:00⟩	Undefined	
UDBB+16	⟨15:00⟩	Undefined	
UDBB+20	⟨15:00⟩	Undefined	
UDBB+22	⟨15:00⟩	Undefined	
UDBB+24	⟨15:00⟩	Undefined	
UDBB+26	⟨15:00⟩	TYPE	The message type field that the DELUA sends in its system ID frame. The value is 260 hex. This is a read-only field.
UDBB+30	⟨15:00⟩	CCOUNT	Character Count – The character count field that the DELUA sends in its system ID frame. This number should be 28 decimal plus the number of bytes in the additional parameters field in words UDBB+66 – UDBB+306.
UDBB+32	⟨15:08⟩	MBZ	Zeros.
UDBB+32	⟨07:00⟩	CODE	Code – The code field that the DELUA sends in its system ID frame. The value is 7 indicating that the frame is a system ID frame. This is a read-only field.
UDBB+34	⟨15:00⟩	RECNUM	Receipt Number – The receipt number field that the DELUA sends in its normal system ID frame. The value is 0.

Table 4-20 Read/Write System ID Parameters UDB Bit Format (Cont)

Word	Bits	Field	Description
			When the DELUA sends a system ID frame in response to a request ID frame from another node, the DELUA includes the receipt number from the request ID frame. Such special receipt numbers cannot be read by the host. This is a read-only field.
UDBB+36	⟨15:00⟩	MVTYPE	MOP Version Type – The MOP version type field that the DELUA sends in its system ID frame. The value is 1. This is a read-only field.
UDBB+40	⟨15:08⟩	MVVER	MOP Version-Version – The MOP version-version field that the DELUA sends in its system ID frame. The value is 3. This is a read-only field.
UDBB+40	⟨07:00⟩	MVLEN	MOP Version Length – The MOP version length field that the DELUA sends in its system ID frame. The value is 3. This is a read-only field.
UDBB+42	⟨15:08⟩	MVUECO	MOP Version User ECO – The MOP version user ECO field that the DELUA sends in its system ID frame. The value is 0. This is a read-only field.
UDBB+42	⟨07:00⟩	MVECO	MOP Version ECO – The MOP version ECO field that the DELUA sends in its system ID frame. The value is 0. This is a read-only field.
UDBB+44	⟨15:00⟩	FTYPE	Function Type – The function type field that the DELUA sends in its system ID frame. The value is 2. This is a read-only field.
UDBB+46	⟨15:08⟩	FVAL1	Function Value 1 – The function value 1 field that the DELUA sends in its system ID frame. The value is 15 hex if the boot select switches are set to enable remote boots, and 5 if remote boots are disabled. This is a read-only field.
UDBB+46	⟨07:00⟩	FLEN	Function Length – The function length field that the DELUA sends in its system ID frame. The value is 2. This is a read-only field.
UDBB+50	⟨15:08⟩	HATYPE ⟨07:00⟩	Byte 0 of the hardware address type field that the DELUA sends in its system ID frame. The value is 7. This is a read-only field.
UDBB+50	⟨07:00⟩	FVAL2	Function Value 2 – The function value 2 field that the DELUA sends in its system ID frame. The value is 0. This is a read-only field.

Table 4-20 Read/Write System ID Parameters UDB Bit Format (Cont)

Word	Bits	Field	Description
UDBB+52	⟨15:08⟩	HALEN	Hardware Address Length – The hardware address length field that the DELUA sends in its system ID frame. The value is 6. This is a read-only field.
UDBB+52	⟨07:00⟩	HATYPE ⟨15:08⟩	Byte 1 of the hardware address type field that the DELUA sends in its system ID frame. The value is 0. This is a read-only field.
UDBB+54	⟨15:00⟩	HA⟨15:00⟩	Word 0 of the hardware address field that the DELUA sends in its system ID frame. This is the Ethernet physical address assigned to the DELUA during manufacture. This is a read-only field.
UDBB+56	⟨15:00⟩	HA⟨31:16⟩	Word 1 of the hardware address field that the DELUA sends in its system ID frame. This is the Ethernet physical address assigned to the DELUA during manufacture. This is a read-only field.
UDBB+60	⟨15:00⟩	HA⟨47:32⟩	Word 2 of the hardware address field that the DELUA sends in its system ID frame. This is the Ethernet physical address assigned to the DELUA during manufacture. This is a read-only field.
UDBB+62	⟨15:00⟩	DTYPE	Device Type – The device type field that the DELUA sends in its system ID frame. The value is 64 hex. This is a read-only field.
UDBB+64	⟨15:08⟩	DVALUE	Device Value – The device value field that the DELUA sends in its system ID frame. The value is 11 decimal. This is a read-only field.
UDBB+64	⟨08:00⟩	DLEN	Device Length – The device length field that the DELUA sends in its system ID frame. The value is 1. This is a read-only field.
UDBB+66 – UDBB+306	⟨15:00⟩	PARAM	Additional Parameters – Up to 146 bytes of data that the DELUA sends in the parameters field of the system ID frame described in Section 5.9. The length of this parameter list is determined by the PLTLEN field in word PCBB+6 of this ancillary function.

4.5.13 Read/Write Load Server Address, Ancillary Function Codes 24/25

These ancillary functions are used to read or change the load server address. When the DELUA receives a boot frame from another node on the network, it loads the host operating system. The boot frame is described in Section 5.1. The load server address is the Ethernet physical address of the preferred network node from which the DELUA should get its host's operating system. The default load server address is the load server multicast address.

Figure 4-22 shows the bit format, and Table 4-21 describes the bit functions.

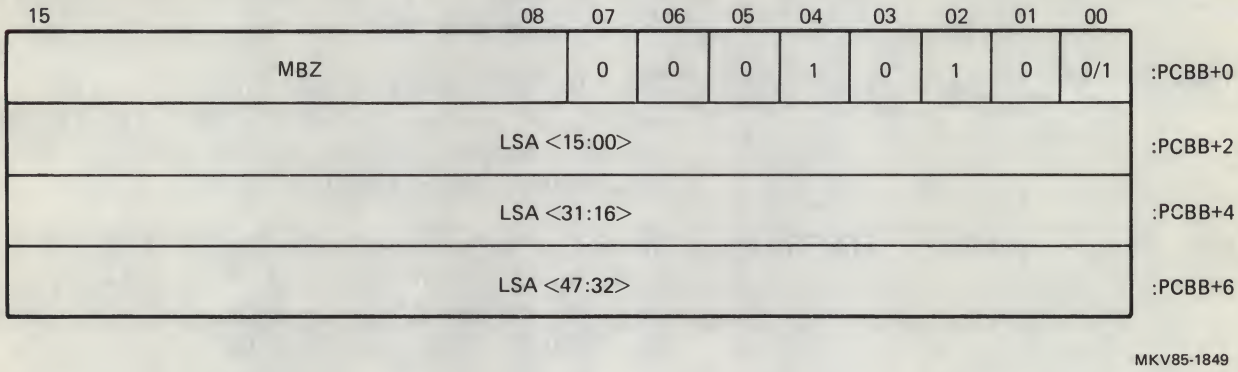


Figure 4-22 Read/Write Load Server Address, Ancillary Function Codes 24/25 Bit Format

Table 4-21 Read/Write Load Server Address, Ancillary Function Codes 24/25 Bit Descriptions

Word	Bits	Field	Description
PCBB+0	⟨15:08⟩	MBZ	Must be zero.
PCBB+0	⟨07:00⟩	OP CODE	Op code = 24 – Read load server address.
			Op code = 25 – Write load server address.
PCBB+2	⟨15:00⟩	LSA ⟨15:00⟩	The low-order 16 address bits of the load server address.
PCBB+4	⟨15:00⟩	LSA ⟨31:16⟩	The middle-order 16 address bits of the load server address.
PCBB+6	⟨15:00⟩	LSA ⟨47:32⟩	The high-order 16 address bits of the load server address.

4.6 TRANSMIT DESCRIPTOR RING ENTRY

A transmit descriptor ring entry points to a data buffer that the port driver wants the DELUA to send on the network. It specifies the size and starting address of the data buffer. After the DELUA sends the data, it writes status information in the transmit descriptor ring entry. The port driver points to the base address of the transmit descriptor ring (TDRB) with the write descriptor ring format, ancillary function code 11.

Figure 4-23 shows the bit format, and Table 4-22 describes the bit functions of an entry in the transmit descriptor ring.

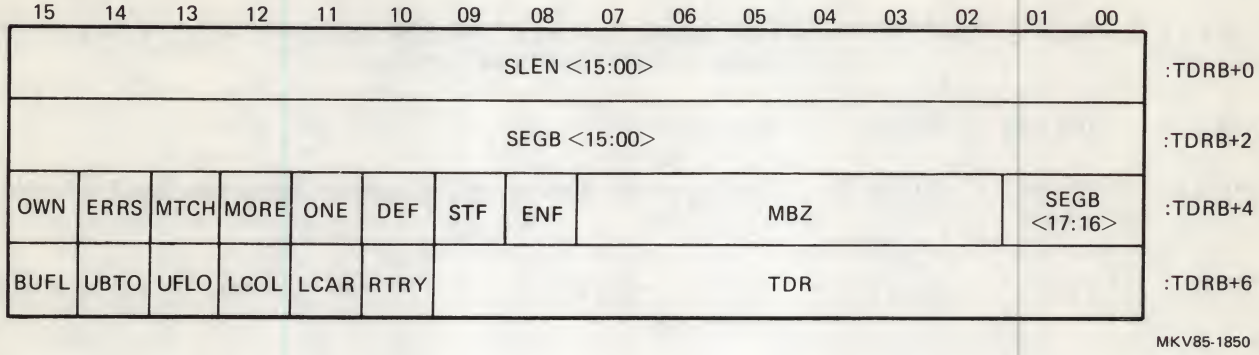


Figure 4-23 Format of an Entry in the Transmit Descriptor Ring

Table 4-22 Bit Descriptions of a Transmit Descriptor Ring Entry

Word	Bit(s)	Field	Description
TDRB+0	⟨15:00⟩	SLEN	Segment Length – Length of the transmit data buffer in bytes.
TDRB+2	⟨15:00⟩	SEGB	The low-order 16 address bits of the segment pointed to by the descriptor.
TDRB+4	⟨15⟩	OWN	Port Ownership – Set by the host to indicate that the DELUA owns the ring entry and should transmit the data buffer on the network. Cleared by the DELUA after it has transmitted the frame and written status into the descriptor ring entry.
TDRB+4	⟨14⟩	ERRS	Error Summary – The logical OR of BUFL ⟨15⟩, UBTO ⟨14⟩, UFLO ⟨13⟩, LCOL ⟨12⟩, LCAR ⟨11⟩, and RTRY ⟨10⟩ in word TDRB+6.
TDRB+4	⟨13⟩	MTCH	Station Match – Set by the DELUA when the destination address of the frame matches the physical address, the broadcast address, or a multicast address of the DELUA. Indicates that the DELUA would have received this message if it had not been transmitting at the same time.
TDRB+4	⟨12⟩	MORE	Multiple Retries Needed – Set by the DELUA when more than one (and up to 16) retries were needed to transmit a frame.
TDRB+4	⟨11⟩	ONE	One Collision – Set by the DELUA when exactly one retry was needed to transmit a frame.
TDRB+4	⟨10⟩	DEF	Deferred – Set when the DELUA had to wait for another node to finish transmitting a frame before the DELUA could transmit this frame.
TDRB+4	⟨09⟩	STF	Start of Frame – Set by the host to indicate that this data buffer is the first data buffer of the frame.

Table 4-22 Bit Descriptions of a Transmit Descriptor Ring Entry (Cont)

Word	Bit(s)	Field	Description
TDRB+4	⟨08⟩	ENF	End of Frame – Set by the host to indicate that this data buffer is the last data buffer of the frame.
TDRB+4	⟨07:02⟩	MBZ	Must be zero.
TDRB+4	⟨01:00⟩	SEGB	The high-order two address bits of the segment pointed to by the descriptor.
TDRB+6	⟨15⟩	BUFL	Buffer Length Error – Set by one or more of the following conditions: 1. The total length of the frame, including chained buffers, is less than the length of the minimum allowable frame. This is 14 bytes if transmit pad enable (TPAD) bit ⟨12⟩ is set in word PCBB+2 of the write mode register, ancillary function code 15. If the DELUA is not in the data padding mode, the minimum length is 60 bytes. If disable transmit CRC (DTCR) bit ⟨03⟩ is set in word PCBB+2 of the write mode register, ancillary function code 15, the minimum length is 64 bytes. 2. The total length of the frame, including chained buffers, exceeds the length of the maximum allowable frame, 1514 bytes. If disable transmit CRC (DTCR) bit ⟨03⟩ is set in word PCBB+2 of the write mode register, ancillary function code 15, then the maximum length is 1518 bytes. 3. The DELUA was in data chaining mode and found an entry with the STF bit set, but it encountered a buffer it did not own before finding a buffer with the ENF bit set. The DELUA sets the BUFL bit in the transmit descriptor ring entry before the entry it does not own. 4. The DELUA was in the data chaining mode and found an entry with the STF bit set, but it encountered another buffer with the STF bit set before finding a buffer with the ENF bit set. The DELUA sets the BUFL bit in the transmit descriptor ring entry before the second entry with the STF bit set. The DELUA does not transmit the frame if BUFL is set for one or more of the buffers that make up the frame.
+6	⟨14⟩	UBTO	UNIBUS Timeout – A UNIBUS timeout was encountered while accessing the buffer pointed to by the descriptor ring entry. Transmission of the frame does not occur if UBTO is set for one of the buffers that make up the frame.

Table 4-22 Bit Descriptions of a Transmit Descriptor Ring Entry (Cont)

Word	Bit(s)	Field	Description
TDRB+6	⟨13⟩	UFLO	Underflow Error – Indicates that the transmitter has truncated a frame. The LANCE system was unable to fetch data words from internal memory fast enough to keep up with the transmit data rate.
TDRB+6	⟨12⟩	LCOL	Late Collision – A collision occurred after all nodes on the network should have known that there was a frame being transmitted. Suggests that the collision detection circuitry of some node may have failed.
TDRB+6	⟨11⟩	LCAR	Loss of Carrier – The carrier was not present on the channel during transmission, indicating a "shorted" cable, the carrier was lost during transmission, or a faulty carrier detect circuit exists.
TDRB+6	⟨10⟩	RTRY	Retry – Transmitter has failed in 16 attempts to transmit the frame due to collisions on the medium.
TDRB+6	⟨09:00⟩	TDR	Time Domain Reflectometry Value – Indicates the amount of time between the start of transmission and the detection of the collision. This value indicates the distance down the cable to the reflective point if the collision is due to the transmitted frame reflecting back from a point of impedance mismatch in the network cable and colliding with itself. Valid only when RTRY ⟨10⟩ is set.

4.7 RECEIVE DESCRIPTOR RING ENTRY

A receive descriptor ring entry points to a data buffer into which the DELUA places a frame that it receives on the network. It specifies the size and starting address of the data buffer. After the DELUA receives a frame and writes it into the data buffer, it writes status information in the receive descriptor ring entry. The port driver points to the base address of the receive descriptor ring (RDRB) with the write descriptor ring format, ancillary function code 11.

Figure 4-24 shows the bit format, and Table 4-23 describes the bit functions of an entry in the receive descriptor ring.

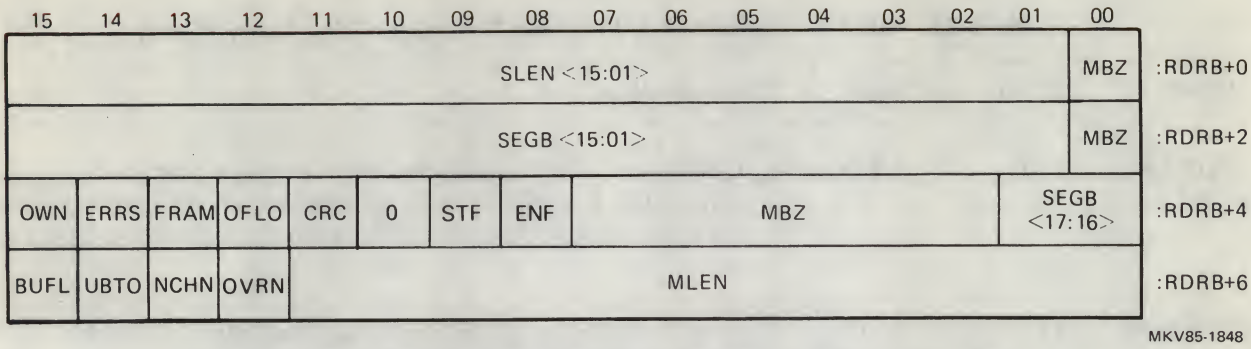


Figure 4-24 Format of an Entry in the Receive Descriptor Ring

Table 4-23 Bit Descriptions of a Receive Descriptor Ring Entry

Word	Bits	Field	Description
RDRB+0	⟨15:01⟩	SLEN	Segment Length – Length of the receive data buffer in bytes.
RDRB+2	⟨15:01⟩	SEGB	The low-order 16 address bits of the segment pointed to by the descriptor.
RDRB+4	⟨15⟩	OWN	Port Ownership – Set by the host to indicate that the DELUA owns the ring entry and can use the associated data buffer to store a frame that it may receive on the network. Cleared by the DELUA after it has received a frame and written it into the data buffer and written status into the descriptor ring entry.
RDRB+4	⟨14⟩	ERRS	Error Summary – The logical OR of FRAM ⟨13⟩ and CRC ⟨11⟩ in word RDRB+4 and BUFL ⟨15⟩, UBTO ⟨14⟩, and OVRN ⟨12⟩ in word RDRB+6.
RDRB+4	⟨13⟩	FRAM	Frame Error – Indicates that the length of the frame is not a multiple of 8 bits.
RDRB+4	⟨12⟩	OFLO	Frame Overflow – The frame received was longer than the maximum allowable Ethernet frame of 1500 data bytes. Data chaining was not attempted and, therefore, the frame may be truncated to fit in the buffer.
RDRB+4	⟨11⟩	CRC	Cyclical Redundancy Check – Frame check error, data is not valid.
RDRB+4	⟨10⟩	MBZ	Must be zero.
RDRB+4	⟨09⟩	STF	Start of Frame – Set by the DELUA to indicate that this data buffer is the first data buffer of the frame.
RDRB+4	⟨08⟩	ENF	End of Frame – Set by the DELUA to indicate that this data buffer is the last data buffer of the frame.
RDRB+4	⟨07:02⟩	MBZ	Must be zero.

Table 4-23 Bit Descriptions of a Receive Descriptor Ring Entry (Cont)

Word	Bits	Field	Description
RDRB+4	⟨01:00⟩	SEGB ⟨17:16⟩	The high-order two address bits of the segment pointed to by the descriptor.
RDRB+6	⟨15⟩	BUFL	Buffer Length Error – The frame does not fit in the current receive buffer and the DELUA does not own the next buffer. The DELUA has truncated the message to fit into the current buffer.
RDRB+6	⟨14⟩	UBTO	UNIBUS Timeout – A UNIBUS timeout was encountered while moving data into the buffer pointed to by the descriptor entry.
RDRB+6	⟨13⟩	NCHN	No Data Chaining – Indicates that disable receive data chaining (DRDC) bit ⟨13⟩ in word PCBB+2 of the write mode register, ancillary function code 15 was set. The frame may be truncated to fit in the single buffer.
RDRB+6	⟨12⟩	OVRN	Overrun Error – The DELUA lost part or all of the frame because the LANCE system was unable to write the data into internal memory as fast as it received the frame from the network.
RDRB+6	⟨11:00⟩	MLEN	Message Length – The total length of the frame that the DELUA received. This field is only valid in the entry in which ENF ⟨08⟩ of word RDRB+4 is set.

4.8 TRANSMIT DATA BUFFER FORMAT

Transmit data buffers may begin on arbitrary byte boundaries. Figure 4-25 shows the format of a buffer when it starts on an odd-byte boundary. Figure 4-26 shows the format of a buffer when it starts on an even-byte boundary.

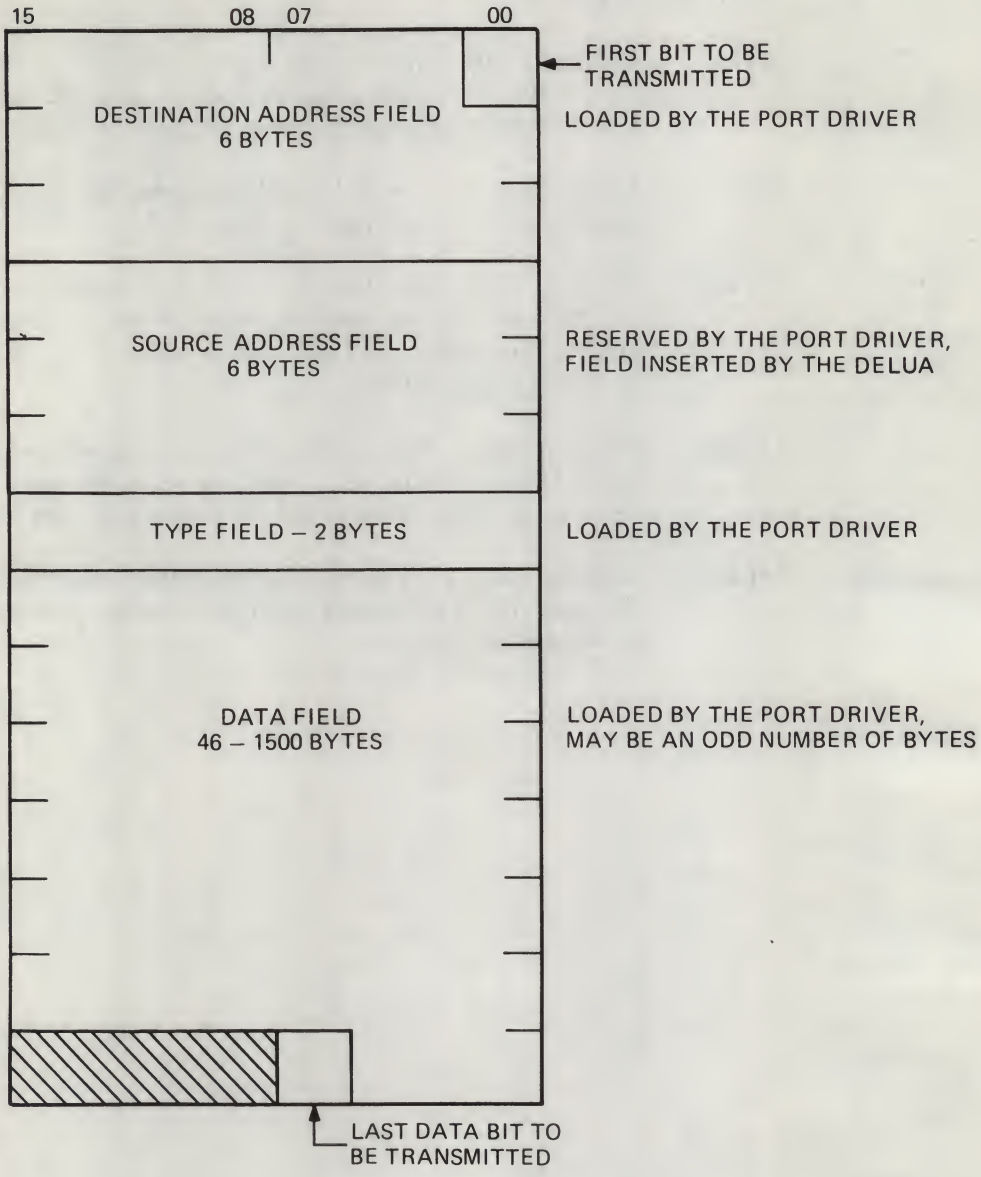


Figure 4-25 Transmit Data Buffer Starting on an Even-Byte Boundary

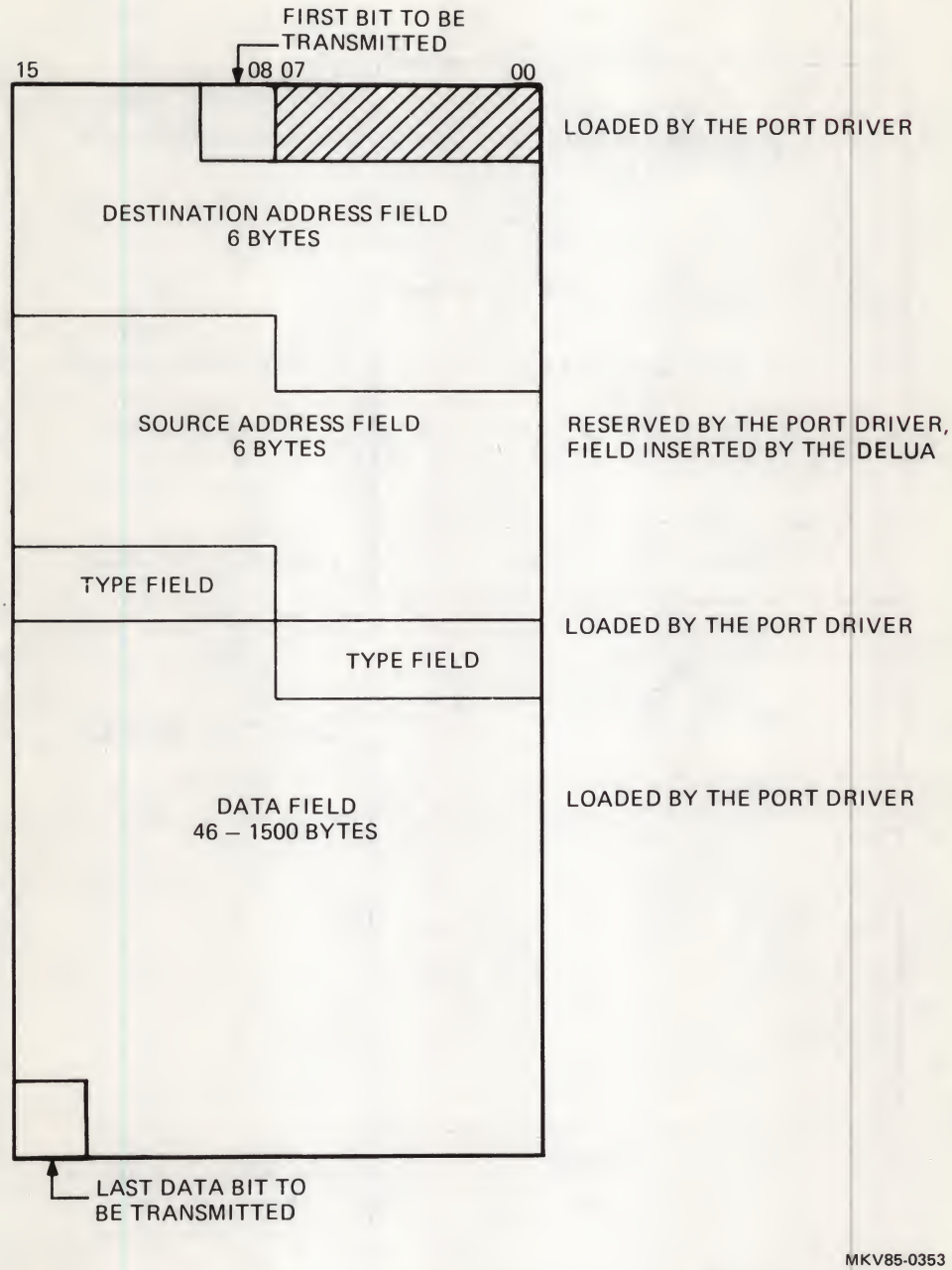


Figure 4-26 Transmit Data Buffer Starting on an Odd-Byte Boundary

4.9 RECEIVE DATA BUFFER FORMAT

Receive data buffers must begin on an even-byte boundary. Figure 4-27 shows the format of a receive data buffer.

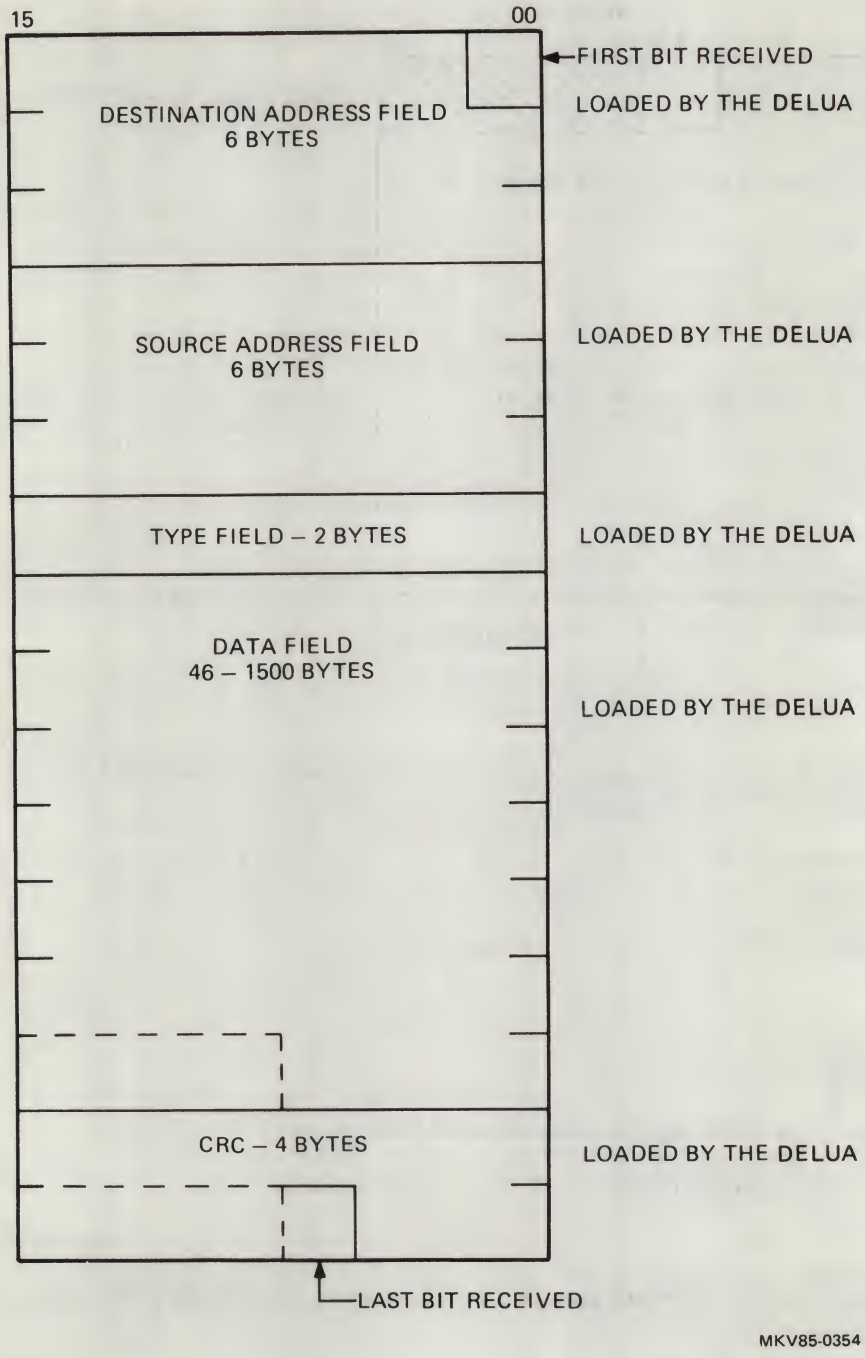


Figure 4-27 Receive Data Buffer Format

CHAPTER 5
MAINTENANCE OPERATIONS

5.1 REMOTE BOOT AND DOWN-LINE LOAD

The remote boot and down-line load features of the DELUA allow the PDP-11 system, in which the DELUA is installed, to be booted by another node on the network. Switch settings on the DELUA module determine whether the DELUA loads the host by transferring the operating system across the network from another node, or the DELUA signals the host to load itself from its own mass storage system. With the optional M9312 boot module and ROM set (order number MR11K-AE), the DELUA loads the host operating system by transferring the operating system across the network from another node during powerup. The DELUA cannot load a VAX host.

5.1.1 Remote Boot Disabled

When remote boot is disabled, the DELUA ignores any boot frames on the network and, thus, cannot be booted by another node.

Remote booting is disabled when the switches on the switch pack at E69 (see Figure 2-6) are configured as follows:

E69 switch 2 (BOOT SEL 0) = ON
E69 switch 3 (BOOT SEL 1) = ON

or

E69 switch 2 (BOOT SEL 0) = OFF
E69 switch 3 (BOOT SEL 1) = OFF

5.1.2 Remote Boot from System Boot ROM

When remote boot from system boot ROM is selected, the DELUA boots its host system by starting the system boot module when it receives a boot frame from another node on the network.

Remote boot from system boot ROM is enabled when the switches on the switch pack at E69 (see Figure 2-6) are configured as follows:

E69 switch 2 (BOOT SEL 0) = ON
E69 switch 3 (BOOT SEL 1) = OFF

The system boot module must be set up to boot on powerup.

The following sequence of events occurs when a boot frame is received from another node on the network.

1. The DELUA receives a boot frame, that is, a frame having the remote console value in its type field and the boot value in its code field.

2. If disable maintenance message (DMNT) bit ⟨09⟩ of word PCBB+2 of the mode register is set, the frame is discarded.

3. If the CRC is invalid and the DELUA is in the running state, the frame is treated as a normal frame and sent to the host. If the CRC is invalid and the DELUA is not in the running state, the frame is discarded. Otherwise, boot processing of the frame continues.

4. If the character count, processor, control, and software ID fields of the boot frame are within expected limits, boot processing of the frame continues. Otherwise, the frame is discarded.

5. The DELUA compares the verification code in the boot frame with the verification code last supplied by the port driver. The port driver writes the verification code with the write system ID parameters, ancillary function code 23. If the code does not match, the DELUA ignores the boot frame. If the port driver has not supplied a verification code or has supplied a code of 0, the DELUA accepts any verification code.

6. The DELUA asserts and releases ACLO on the UNIBUS, which starts the system boot module.

7. The DELUA ignores any additional boot frames on the network for 40 seconds to give the system time to start.

5.1.3 Remote Boot and System Load

When remote boot and system load is selected, the DELUA loads the host with an operating system transferred from another node on the network when it receives a boot message from another node.

Remote boot and system load is enabled when the switches on the switch pack at E69 (see Figure 2-6) are configured as follows:

E69 switch 2 (BOOT SEL 0) = OFF
E69 switch 3 (BOOT SEL 1) = ON

The system processor must be set up so that it does not boot on powerup.

The following sequence of events occurs when a boot frame is received from another node on the network.

1. The DELUA receives a boot frame, that is, a frame having the remote console value in its type field and the boot value in its code field.

2. If disable maintenance message (DMNT) bit ⟨09⟩ of word PCBB+2 of the mode register is set, the frame is discarded.

3. If the CRC is invalid and the DELUA is in the running state, the frame is treated as a normal frame and sent to the host. If the CRC is invalid and the DELUA is not in the running state, the frame is discarded. Otherwise, boot processing of the frame continues.

4. If the character count, processor, control, and software ID fields of the boot frame are within expected limits, boot processing of the frame continues. Otherwise, the frame is discarded.

5. The DELUA compares the verification code in the boot frame with the verification code last supplied by the port driver. The port driver writes the verification code with the write system ID parameters, ancillary function code 23. If the code does not match, the DELUA ignores the boot frame. If the port driver has not supplied a verification code or has supplied a code of 0, the DELUA accepts any verification code.

6. The DELUA decodes the processor field of the boot frame to determine whether to request system processor type software or communication processor type software.

7. The DELUA enters the primary load state and sets the unsolicited state change interrupt (USCI) bit ⟨08⟩ of PCSR0.

8. To keep the host busy and prevent it from interfering with the operating system load, the DELUA forces the host into executing a branch self instruction in memory address 2. To accomplish this, the DELUA loads the following program into host memory:

2/	777	Branch self
4/	PCSR0 address of the DELUA	
6/	0	
10/	12	
12/	0	
14/	16	
16/	0	
20/	22	
22/	0	
24/	30	Powerup at location 30
26/	340	Set priority to 7
30/	012706	Set up the stack pointer 1000
32/	1000	to avoid stack limit traps
34/	762	Branch to location 2 to do Branch self

9. The DELUA asserts the ACLO signal on the UNIBUS, which causes the host processor to perform a power-fail trap. This causes the host to read the processor status word from location 26 and jump to the address in location 24. After a few instructions, the host is stuck on the branch self instruction at address 2. The DELUA blocks UNIBUS INIT to itself.

10. The DELUA forms a request program frame. The DELUA copies the software ID field of the boot frame into the software ID field of the request program frame. The DELUA copies the address in the source address field of the boot frame to the destination address field of the request program frame if bit ⟨00⟩ of the control field of the boot frame equals 1. If bit ⟨00⟩ of the control field of the boot frame equals 0, the DELUA writes the load server address into the destination address field of the request program frame. The host sets the load server address with the write load server address, ancillary function code 25. If the host has not set the load server address, the DELUA uses the load assistant multicast address.

11. The DELUA transmits the request program frame and waits for a memory load with transfer address frame. The memory load with transfer address frame contains the secondary loader program.

12. If, after 5 seconds, the DELUA receives an incorrect memory load with transfer address frame, or does not receive any memory load with transfer address frame, it retransmits the request program frame. The DELUA repeats this procedure up to eight times. During this time, the DELUA discards any incoming boot frame. If the DELUA does not receive a memory load with transfer address frame after eight tries, it takes the following action:

    a. If the boot message instructed the DELUA to request communication processor type software, the DELUA enters the ready state and sets the unsolicited state change interrupt (USCI) bit ⟨08⟩ of PCSR0.

    b. If the boot message instructed the DELUA to request system processor type software, it changes the software ID field of the request program frame to zero (to ask for any type of system processor software) and it changes the destination address field to the load assistant multicast address. The DELUA sends this request program frame every 30 seconds until it receives a memory load with transfer address frame. During this time the DELUA accepts any incoming boot frame.

13. The DELUA receives a memory load with transfer address frame. If the DELUA transmitted the request program frame to a specific node, then it will only accept a memory load with transfer address frame from that node. If the DELUA transmitted the request program frame to a multicast address, then it will accept any error-free memory load with transfer address frame.

14. The memory load with transfer address frame contains the secondary loader program. The DELUA loads the data field of the memory load with transfer address frame into its memory starting at the load address supplied in the frame.

15. The DELUA starts the secondary loader program by jumping to the transfer address supplied in the memory load with transfer address frame.

16. The secondary loader program requests a tertiary loader program from another node, loads it into host memory, and starts it.

17. The tertiary loader program in host mémory contains a DELUA port driver program. It resets and initializes the DELUA and uses it to transfer an operating system into the host from another node. The tertiary loader program then starts the host operating system.

5.1.4 Remote Boot on Powerup

A PDP-11 system can be set up so that the DELUA performs a remote boot when the system powers up. You must install an M9312 boot module with ROM set (order number MR11K-AE). You must also set the boot select switches to either remote boot and system load or disable remote boot.

At system powerup, the program code in the boot ROM executes. This program resets the DELUA and then waits for it to finish selftest and enter the ready state. The program sets up a PCB and issues a read default physical address, ancillary function code 2. It prints the Ethernet physical address of the DELUA on the system console terminal. Then it writes a BOOT port command into PCSR0. This causes the DELUA to perform a remote boot as described in Section 5.1.5.

5.1.5 BOOT Port Command

The BOOT port command causes the DELUA to request an operating system from another node on the network, to load the operating system into the host, and start it.

The following events occur when the host writes a BOOT port command into PCSR0.

1. The DELUA receives the BOOT port command.

2. The DELUA enters the primary load state and sets the done interrupt (DNI) bit ⟨11⟩ in PCSR0.

3. The DELUA forms a request program frame. The DELUA writes the software ID field of the request program frame with the SOFTID field bits ⟨07:00⟩ of word UDBB+10 supplied with the last write system ID parameters, ancillary function code 23. The DELUA writes the load server address into the destination address field of the request program frame. The host sets the load server address with the write load server address, ancillary function code 25. If the host has not set the load server address, the DELUA uses the load assistant multicast address.

4. The DELUA transmits the request program frame and waits for a memory load with transfer address frame. The remainder of the BOOT port command sequence is the same as the remote boot and system load sequence described in Section 5.1.3. It is assumed that the host processor will be in an appropriate state so that it will not interfere with loading and starting the tertiary loader program.

5.2 BOOT FRAME FORMAT

Figure 5-1 shows each byte in the boot frame, and Table 5-1 describes the function of each byte.

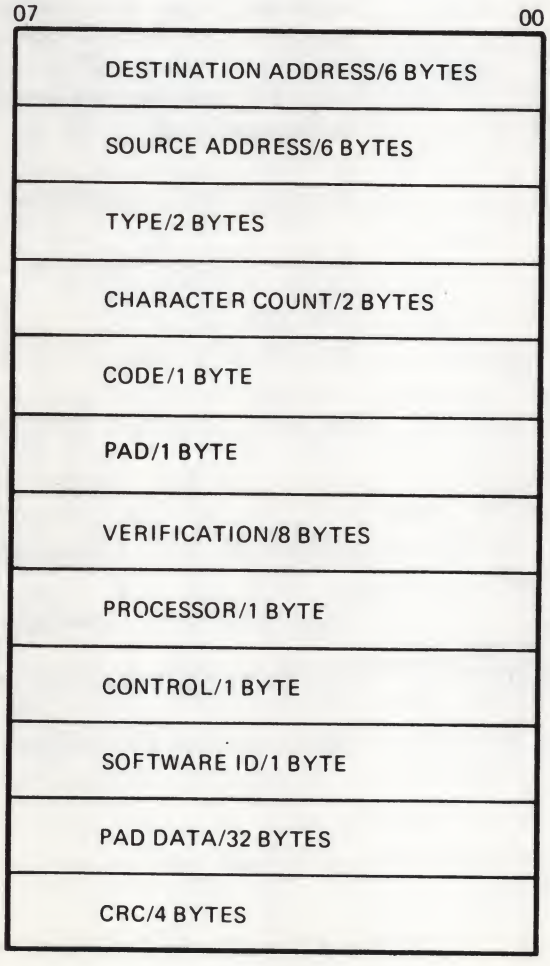


Figure 5-1 Boot Frame Format

Table 5-1 Boot Frame Description

Field	Length (Bytes)	Description
Destination Address	6	The physical address of the DELUA.
Source Address	6	The physical address of the requesting station.
Type	2	The remote console type. Value = (0260) 60-02 hex.
Character Count	2	The number of bytes following the character count field, less pad data and CRC. Value = 000D hex.
Code	1	The function code for the boot frame. Value = 06 hex.
PAD	1	The constant 0.
Verification	8	The code to be compared against the port-driver-supplied verification code. The codes must match before the DELUA will honor the boot. If the DELUA has not been supplied with a verification code by the port driver or supplied with a code of 0, the DELUA accepts any value in the boot frame verification field.
Processor	1	Value = 00 hex – System boot, enter the primary load state. Value = 01 hex – Boot the DELUA, enter the primary load state.
Control	1	Bit ⟨00⟩ = 0 – Boot from the system default. Bit ⟨00⟩ = 1 – Boot from the requesting system.
Software ID	1	Value = 00 hex – No ID. Value = FF hex – Operating system. Value = FE hex – Diagnostics.
PAD Data	32	Pad characters, zeros are added to pad the frame to 64 bytes.
CRC	4	Incoming block check character.

5.3 REQUEST PROGRAM FRAME FORMAT

Figure 5-2 shows each byte in the request program frame, and Table 5-2 describes the function of each byte.

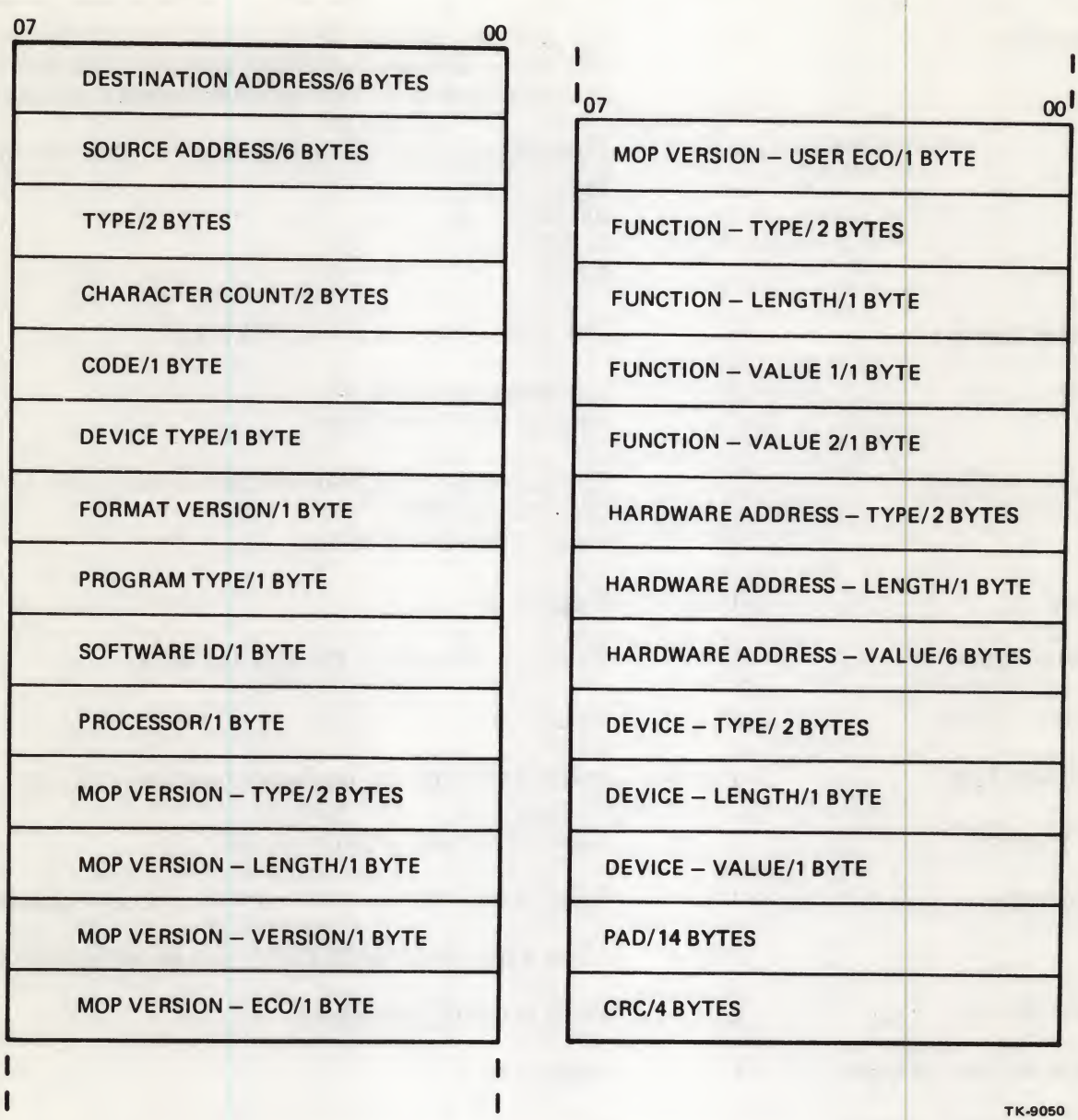


Figure 5-2 Request Program Frame Format

Table 5-2 Request Program Frame Description

Field	Length (Bytes)	Description
Destination	6	The address supplied by the write load server ancillary function or the source address of a received boot frame. The default address is the load assistant multicast address. Load assistant multicast address value = AB-00-00-01-00-00 hex. (00AB) (0100) (0000)
Source Address	6	The physical address of the DELUA.
Type	2	The dump/load type. Value = (0160) 60-01 hex.
Character Count	2	The number of bytes following the character count field, less pad data and CRC. Value = (001E) 1E-00 hex.
Code	1	Value = 08.
Device Type	1	Value = 11 decimal – The DELUA code.
Format Version	1	Value = 01.
Program Type	1	Value = 00, DELUA microcode (secondary loader).
Software ID	1	Value = 0 or any negative number.
Processor	1	Value = 00 – System boot, enter the primary load state. Value = 01 – Boot the DELUA, enter the primary load state.
MOP Version – Type	2	Value = (0001) 01-00 hex.
MOP Version – Length	1	Value = 03.
MOP Version – Version	1	Value = 03.
MOP Version – ECO	1	Value = 00.
MOP Version – User ECO	1	Value = 00.
Function – Type	2	Value = (0002) 02-00 hex.
Function – Length	1	Value = 02.

Table 5-2 Request Program Frame Description (Cont)

Field	Length (Bytes)	Description
Function – Value 1	1	If remote boot is enabled with the boot select switches, then the DELUA supports the following maintenance functions: loop, primary loader, boot. Value = 15 hex. If remote boot is disabled with the boot select switches, then the DELUA supports the following maintenance functions: loop, primary loader. Value = 05 hex.
Function – Value 2	1	Value = 00.
Hardware Address – Type	2	Value = (0007) 07-00 hex.
Hardware Address – Length	1	Value = 06.
Hardware Address – Value	6	The physical address of the DELUA.
Device – Type	2	Value = (0064) 64-00 hex.
Device – Length	1	Value = 01.
Device – Value	1	Value = 11 decimal – The DELUA code.
PAD Bytes	14	14 bytes of zeros to pad the frame to 64 bytes.
CRC	4	DELUA-generated block check character.

5.4 MEMORY LOAD WITH TRANSFER ADDRESS FRAME FORMAT

Figure 5-3 shows each byte in the memory load with transfer address frame, and Table 5-3 describes the function of each byte.

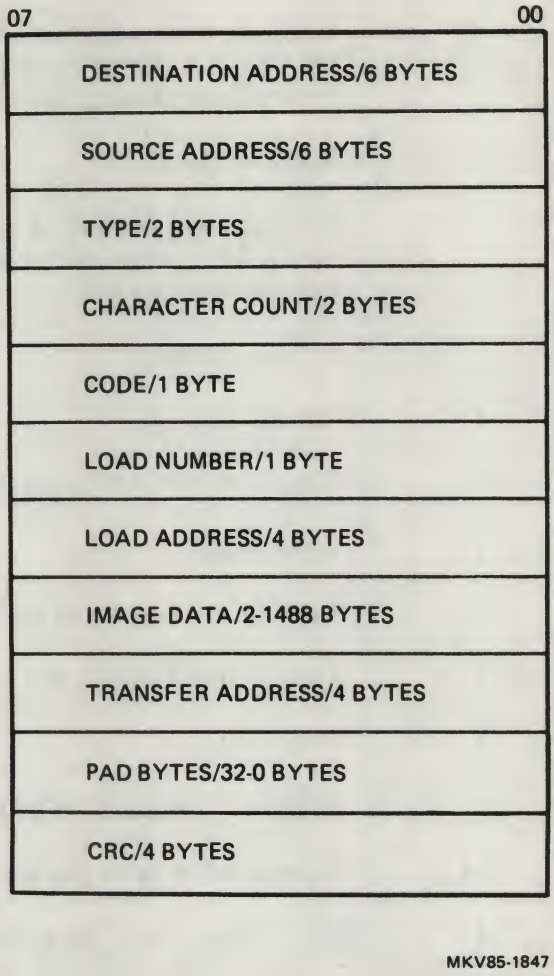


Figure 5-3 Memory Load with Transfer Address Frame Format

Table 5-3 Memory Load with Transfer Address Frame Description

Field	Length (Bytes)	Description
Destination Address	6	The physical address of the DELUA.
Source Address	6	The physical address of the load server.
Type	2	The dump/load type. Value = (0160) 60-01 hex.
Character Count	2	The number of bytes following the character count field, not counting the pad bytes or the CRC. Value = 12 to 1498.
Code	1	Value = 00.
Load Number	1	Value = 00.
Load Address	4	The starting address in DELUA internal memory for storage of the image data.
Image Data	2-1488	The image data of the secondary loader program to be stored in DELUA internal memory.
Transfer Address	4	The internal memory address at which the DELUA starts executing the secondary loader program.
Pad Bytes	32-0	Pad bytes used when necessary to increase length of frame to the 64-byte minimum.
CRC	4	Received block check character.

5.5 INTERNAL AND EXTERNAL LOOPBACK MODE

The DELUA enters loopback mode when LOOP bit ⟨02⟩ is set in word PCBB+2 of the write mode register, ancillary function code 15. If INTL bit ⟨06⟩ is also set, then the LANCE system loops the data internally within the DELUA. If INTL bit ⟨06⟩ is not set, the LANCE system loops the data externally by transmitting the frame on the network and reading it back at the same time.

A loopback frame must be set up just like a normal frame, complete with destination address, source address, type, and data fields. The destination address must be the physical address for the DELUA unit or a broadcast or multicast address that the DELUA is enabled to receive.

The data field can be no larger than 32 bytes, due to the size of the data silo within the LANCE chip. If the disable transmitter CRC (DTCR) bit ⟨03⟩ of the mode register is set, the DELUA does not generate and send the 4-byte CRC field with the loopback frame. It does, however, perform the normal CRC check while it is reading the loopback frame. The port driver must provide a frame with 28 bytes of data and a 4-byte CRC in the data field. If DTCR bit ⟨03⟩ is not set, the DELUA generates a CRC and appends it to the 32 bytes of data, but it does not perform the normal CRC check while it is reading the loopback frame. Thus, the port driver receives 36 bytes of data (32 data bytes plus 4 CRC bytes). It must check that the DELUA hardware generated the correct CRC field.

In external loopback mode, the RUNT frame filter is disabled so that the DELUA is able to receive frames smaller than 64 bytes.

5.6 CHANNEL LOOPBACK

The DELUA microcode supports maintenance operations protocol (MOP) loop operations. Loop frames have the Ethernet configuration test (ECT) in the type field. The DELUA does not check the type field of multicast address frames that it receives. The port driver must check the type field of multicast frames.

The DELUA processes a loopback frame in the following manner:

1. The DELUA receives a loopback frame, that is, a frame having the Ethernet communications test (ECT) type value in its type field.

2. If disable maintenance message (DMNT) bit ⟨09⟩ of word PCBB+2 of the mode register is set, the frame is discarded.

3. If the CRC is invalid and the DELUA is in the running state, the frame is treated as a normal frame and sent to the host. If the CRC is invalid and the DELUA is not in the running state, the frame is discarded. Otherwise, loopback processing continues.

4. If the destination address of the frame is a multicast address and the DELUA is in the running state, the frame is treated as a normal frame and sent to the host. If it contains a multicast address and the DELUA is not in the running state, the frame is discarded.

5. The DELUA locates the function field by adding the value in the skip count field to the location of the skip count field plus 1. If the function value is not 1 or 2 and the DELUA is in the running state, the frame is treated as a normal frame and sent to the host. If the function value is not 1 or 2 and the DELUA is not in the running state, the frame is discarded.

6. If the function value is 1, this indicates that the loopback frame was originally sent by the host and has now been looped back by one or more other nodes. If the DELUA is in the running state, it sends the frame to the host. If the DELUA is not in the running state, the frame is discarded.

7. If the function value is 2, indicating that the DELUA should forward the frame to another node, the DELUA does the following:

    a. Inserts the contents of the forward address field into the destination address field

    b. Replaces the source address field with the physical address of the DELUA

    c. Adds eight to the value of the skip count

    d. Strips the last 4 bytes (the CRC) from the frame

    e. Transmits the resulting frame, generating and appending 4 bytes of CRC

5.7 LOOPBACK FRAME FORMAT

A loopback frame is set up so that it can be forwarded by a series of nodes and then returned to the originating node. The frame contains a list of node addresses with a function code associated with each address. Each address will have the forward function code, which tells the node to forward the frame to the next address on the list. The last address on the list should be the address of the originating node so that the frame will come back to that node. After the last address on the list is an entry with just a reply function code. When the DELUA receives a loopback frame with the reply function code, it passes the frame to the host because this is a loopback frame that originated with the host and has now been returned.

Figure 5-4 shows each byte in the loopback frame, and Table 5-4 describes the function of each byte.

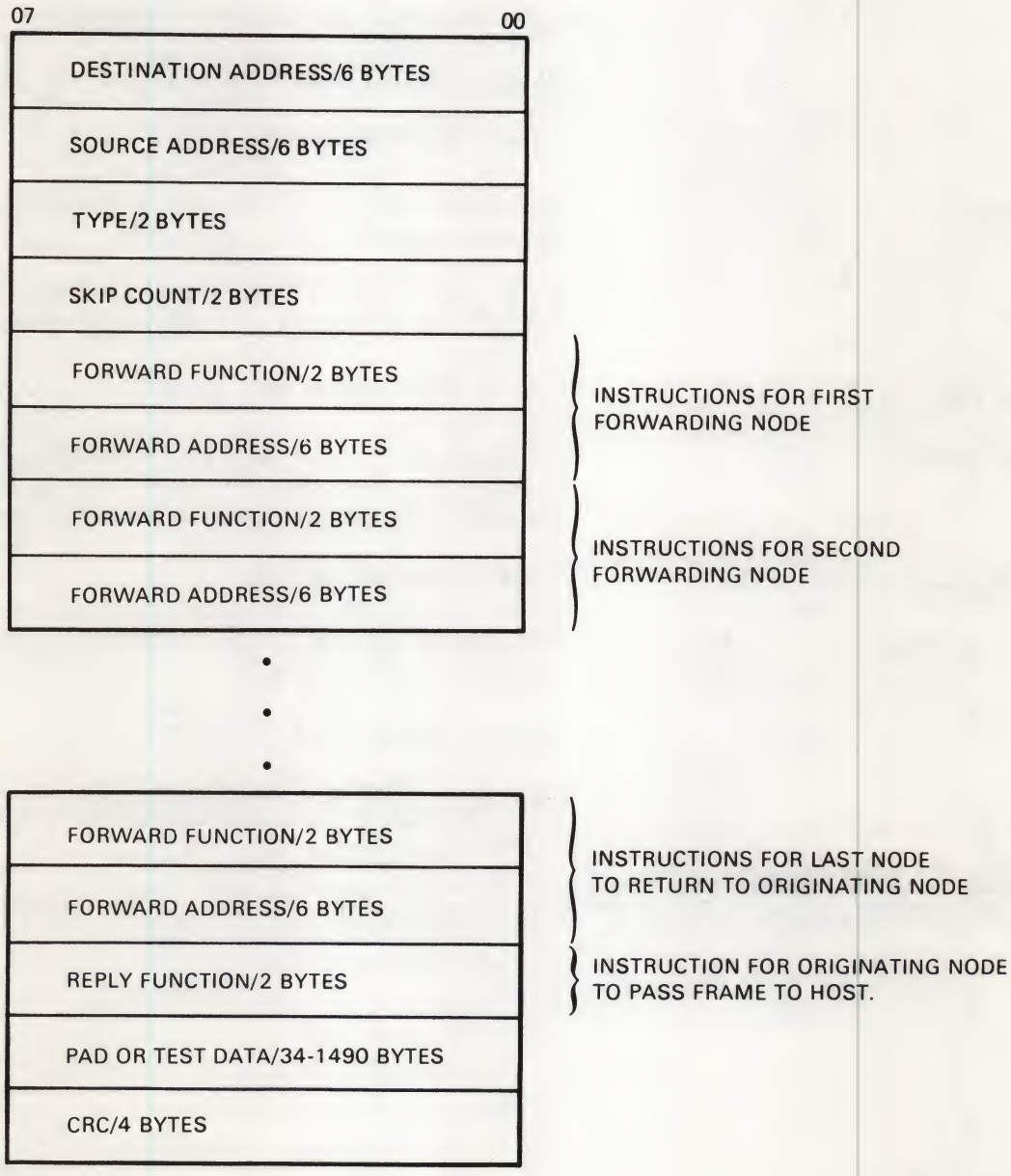


Figure 5-4 Loopback Frame Format

Table 5-4 Loopback Frame Description

Field	Length (Bytes)	Description
Destination Address	6	Inbound – The physical address of the DELUA, or the broadcast address. Outbound – The forward address.
Source Address	6	Inbound – The physical address of the loop requesting station. Outbound – The physical address of the DELUA.
Type	2	Ethernet communications test (ECT) indicating a loopback type frame. Value = (0090) 90-00 hex.
Skip Count	2	The number of bytes to skip after this field to find the appropriate function field. If this field specifies a forward type operation, the DELUA adds 8 to the skip count before transmitting the frame.
Forward Function	2	Value = (0002) 02-00 hex.
Forward Address	6	The physical address of the node to which the frame should be sent next. The DELUA copies this address into the destination address field and then transmits the frame.
Reply Function	2	Value = (0001) 01-00 hex.
Pad or Test Data	34 to 1490	Pad bytes of zeros to increase the frame to 64 bytes or a loopback test data pattern.
CRC	4	Inbound – Block check character. Outbound – CRC generated by the DELUA.

5.8 REQUEST ID FRAME

When the DELUA receives a request ID frame, it sends a system ID frame to the requesting node.

Figure 5-5 shows each byte in the request ID frame, and Table 5-5 describes the function of each byte.

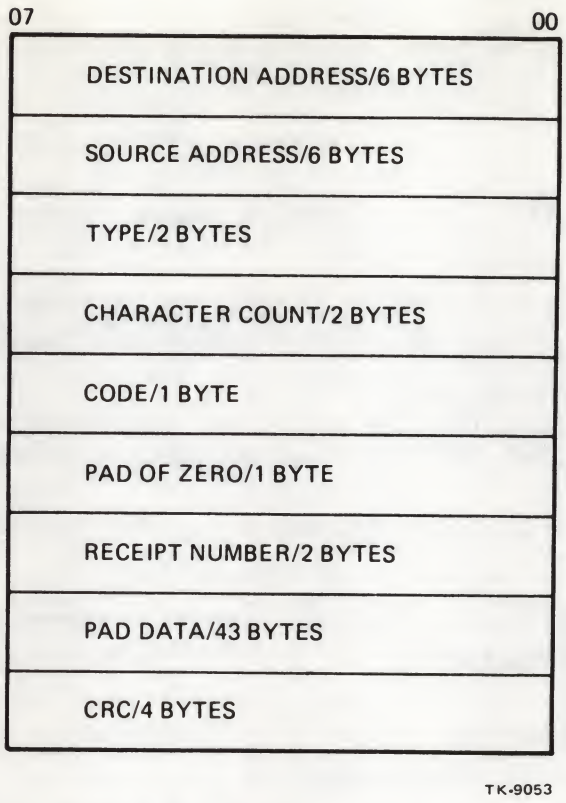


Figure 5-5 Request ID Frame Format

Table 5-5 Request ID Frame Description

Field	Length (Bytes)	Description
Destination Address	6	The physical address of the DELUA.
Source Address	6	The physical address of the requesting station.
Type	2	The remote console type. Value = (0260) 60-02 hex.
Character Count	2	The number of bytes following the character count field, less pad data and CRC. Value = 04 hex.
Code	1	The function code for the request ID frame. Value = 05 hex.

Table 5-5 Request ID Frame Description (Cont)

Field	Length (Bytes)	Description
Pad of Zero	1	Value = 00 hex.
Receipt Number	2	A receipt number to identify the request.
Pad Data	43	Characters inserted, as required, to pad the frame to 64 bytes.
CRC	4	Incoming block check character.

5.9 SYSTEM ID FRAME FORMAT

The DELUA transmits a system ID frame to the remote console service multicast address every 10 minutes. The DELUA also sends a system ID frame to a specific node in response to a request ID frame.

Figure 5-6 shows each byte in the system ID frame, and Table 5-6 describes the function of each byte.

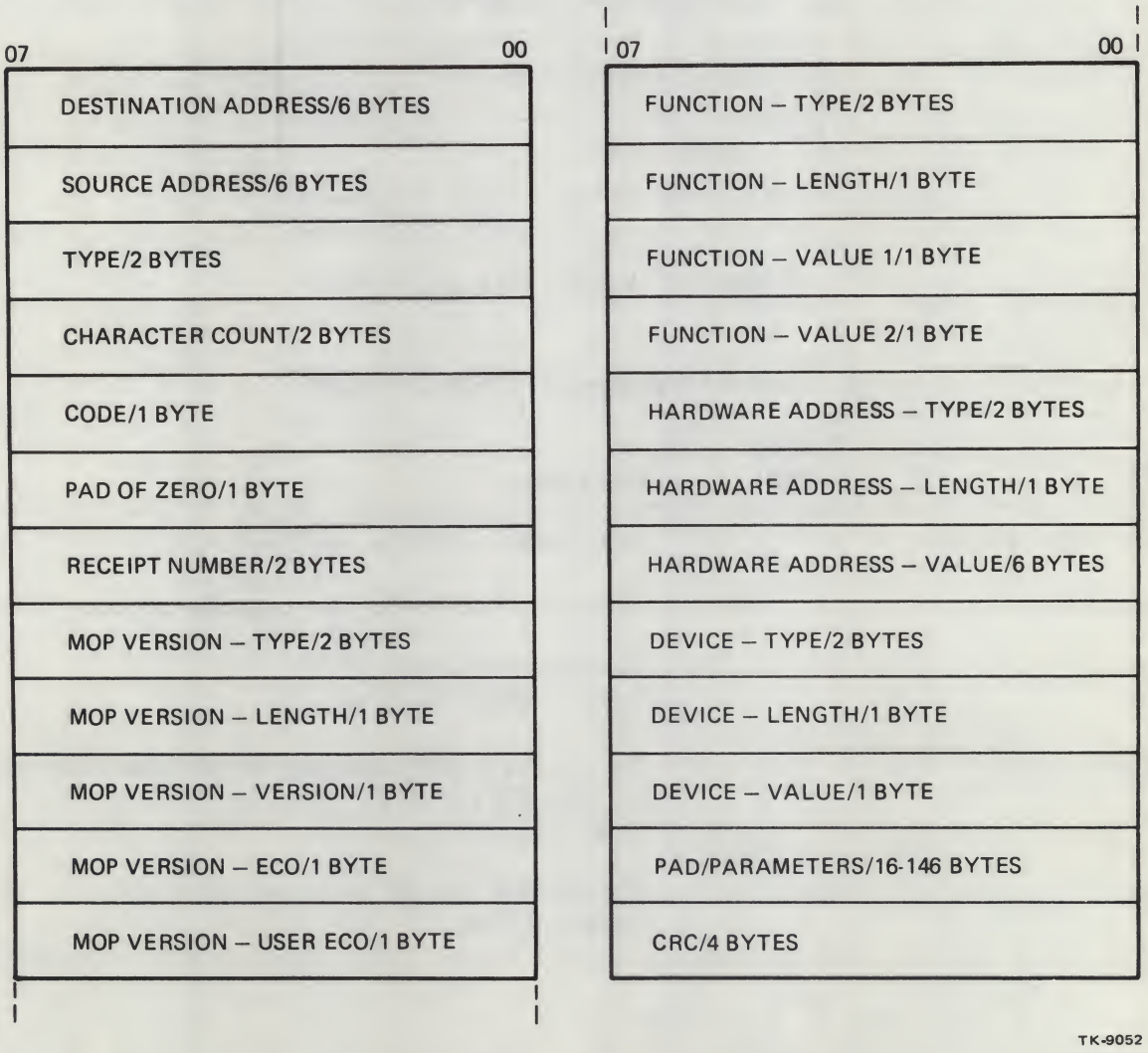


Figure 5-6 System ID Frame Format

Table 5-6 System ID Frame Description

Field	Length (Bytes)	Description
Destination Address	6	The physical address of the ID requesting station or the remote console service multicast address. Remote console service multicast address value = AB-00-00-02-00-00 hex. (00AB) (0200) (0000)
Source Address	6	The physical address of the DELUA.
Type	2	The remote console type. Value = (0260) 60-02 hex.
Character Count	2	The number of bytes following the character count field, less pad data and CRC. Value = (001C) 1C-00 to (05DA) DA-05 hex.
Code	1	The function code for the system ID frame. Value = 07 hex.
Pad of Zero	1	Value = 00 hex.
Receipt Number	2	A receipt number to identify the request.
MOP Version – Type	2	Value = (0001) 01-00 hex.
MOP Version – Length	1	Value = 03 hex.
MOP Version – Version	1	Value = 03 hex.
MOP Version – ECO	1	Value = 00 hex.
MOP Version – User ECO	1	Value = 00 hex.
Function – Type	2	Value = (0002) 02-00 hex.
Function – Length	1	Value = 02 hex.
Function – Value 1	1	If remote boot is enabled with the boot select switches, then the DELUA supports the following maintenance functions: loop, primary loader, boot. Value = 15 hex. If remote boot is disabled with the boot select switches, then the DELUA supports the following maintenance functions: loop, primary loader. Value = 05 hex.

Table 5-6 System ID Frame Description (Cont)

Field	Length (Bytes)	Description
Function – Value 2	1	Value = 00.
Hardware Address – Type	2	Value = (0007) 07-00 hex.
Hardware Address – Length	1	Value = 06 hex.
Hardware Address – Value	6	The default physical address of the DELUA.
Device – Type	2	Value = (0064) 64-00 hex.
Device – Length	1	Value = 01.
Device – Value	1	Value = 11 decimal – the DELUA code.
PAD/Parameters	146	The set of additional parameters supplied by the host in words UDBB+66 through UDBB+306 of the write system ID parameters, ancillary function code 23. If not supplied, the DELUA adds 16 bytes of zeros to pad the frame to 64 bytes.
CRC	4	Outgoing block check character.

5.10 MICROCODE LOADING

To load custom microcode into the DELUA, the port driver must put the DELUA into the port halted state or the ready state by issuing a HALT or STOP port command. When the DELUA is in the halted state, internal memory from address 4400 to 1FFFE is available for loading. When the DELUA is in the ready state, internal memory from address 4400 to 6400 hex is available for loading.

The recommended procedure to load and start microcode is as follows:

1. Reset the DELUA by writing the RESET bit ⟨05⟩ in PCSR0.
2. Wait for the done interrupt bit ⟨11⟩ in PCSR0 to be set and the DELUA to enter the ready state.
3. Write a HALT port command into PCSR0.
4. Wait for the done interrupt bit ⟨11⟩ in PCSR0 to be set and the DELUA to enter the port halted state.
5. Use the load internal memory, ancillary function code 21 to load a block of code into DELUA memory.
6. Use the dump internal memory, ancillary function code 20 to dump the same block of code from internal memory and perform a word-by-word comparison.

7. If the comparison produces no errors, repeat the load, dump and compare until the entire microcode is loaded.

8. Issue the start microaddress, ancillary function code 1 to start the DELUA executing at a specified address.

5.11 MICROCODE UPDATE PROCESS

The DELUA has a provision for accepting updates or patches to its microcode without replacing the ROM containing the microcode. Updates can be included as a part of the DELUA port driver software in new releases of the host's operating system.

If the port driver has a DELUA microcode patch, it loads the patch whenever it initializes the DELUA.

The microcode patch file consists of the standard RSX label blocks followed by data blocks as shown in Figure 5-7.

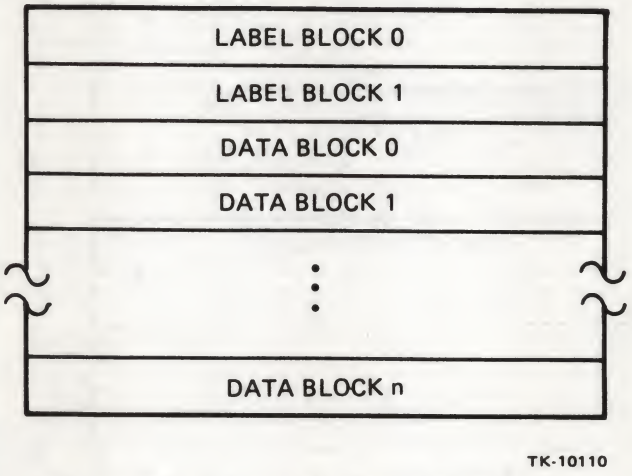


Figure 5-7 Microcode Patch File Format

Figure 5-8 shows the format of data blocks in a patch file. The first word of a data block is a byte count of the number of data bytes to be transferred into the DELUA. The second word is the address to begin loading the data inside the DELUA. Each data block can contain a number of microcode patches. Unused space at the end of a data block must be filled with zeros. No single patch can extend beyond a data block. Large patches must be divided into a series of smaller patches. The two words after the last patch in the file must be a word containing negative one and a word containing the internal starting address to begin microcode execution.

The DELUA must be in the port halted state or the ready state to accept microcode patches. During DELUA initialization, the port driver loads each microcode patch into the DELUA with the load internal memory, ancillary function code 21. The port driver uses the byte count and internal address supplied in the patch file. When the port driver finds a patch in the patch file with a byte count of zero indicating pad data at the end of a data block, it skips to the beginning of the next data block. When the port driver finds a byte count of negative one, it uses the next word as the starting microaddress and issues the start microaddress, ancillary function code 1.

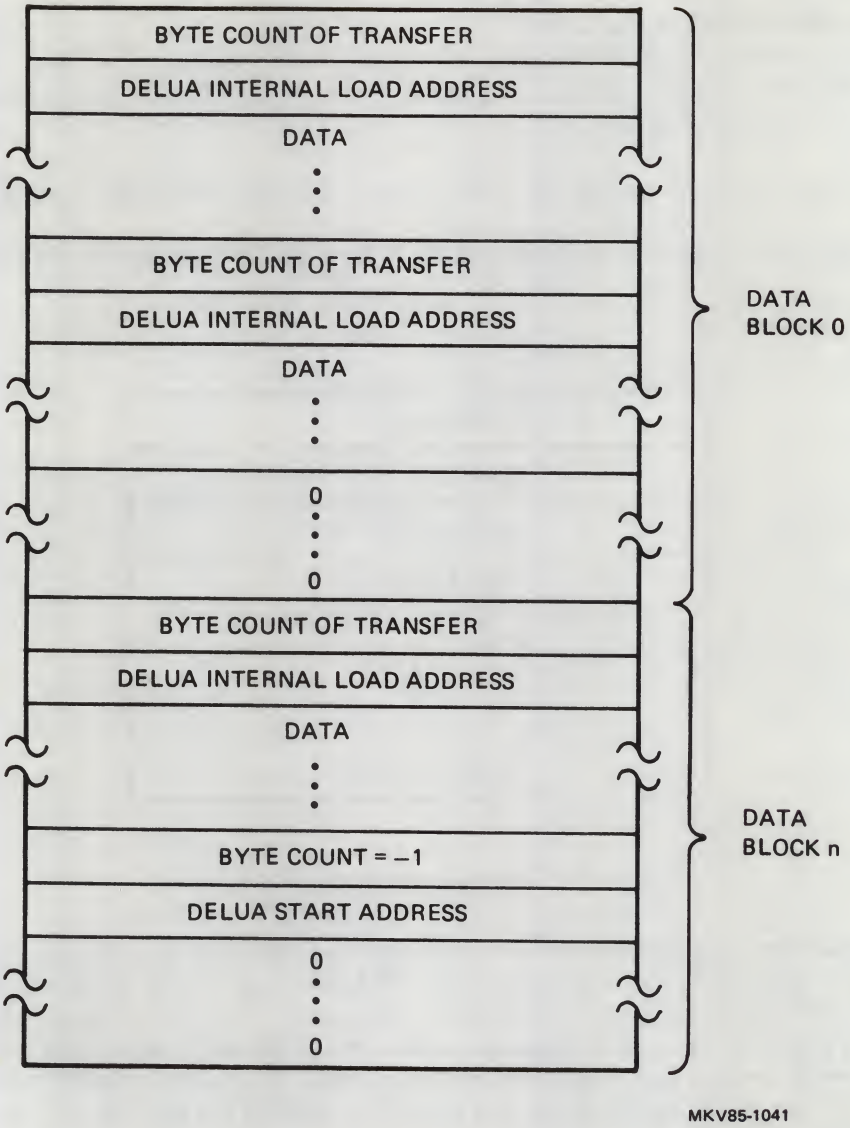


Figure 5-8 Patch File Data Block Format

CHAPTER 6
SERVICE

6.1 MAINTENANCE PHILOSOPHY

The maintenance philosophy for the DELUA is isolation of the field replaceable unit (FRU). The FRUs for the DELUA are the M7521 module, the UNA bulkhead assembly, and the UNA bulkhead cable.

Faults that appear to be in the DELUA can be caused by faults in the network: the transceiver, the transceiver cable, or the network coaxial cable. Faults that are isolated to the network should be referred to network service personnel.

6.2 TROUBLESHOOTING PROCEDURE

The troubleshooting procedure is shown in the flowchart in Figure 6-1.

6.2.1 Selftest

To run the DELUA selftest, turn the power off and then back on. The simplest way to do this is to use the circuit breaker for the cabinet containing the DELUA.

When the test has completed successfully, only one LED, D8, should be on. This indicates that the DELUA is in the ready state. LED D5, the activity indicator, may also be flickering. Figure 6-2 shows the selftest LEDs, and Table 6-1 lists the selftest error and status codes.

The selftest checks the DELUA module's internal circuitry, reads and writes the four UNIBUS registers in the DELUA, and sends messages on the network and reads them back.

If the DELUA fails its external loopback test, check the LED on the UNA bulkhead assembly that monitors the −15 V supply to the transceiver. There is also a circuit breaker on the UNA bulkhead assembly for the −15 V power to the transceiver.

If the LED is on, check for a bad transceiver by attaching an H4080 loopback transceiver (shown in Figure 2-9) and running the test again.

If the external loopback test still fails, replace the FRUs in the following order:

1. The UNA bulkhead cable
2. The UNA bulkhead assembly
3. The DELUA module (M7521)

If the DELUA selftest fails any test other than the external loopback test, the most likely failure is within the DELUA module (M7521).

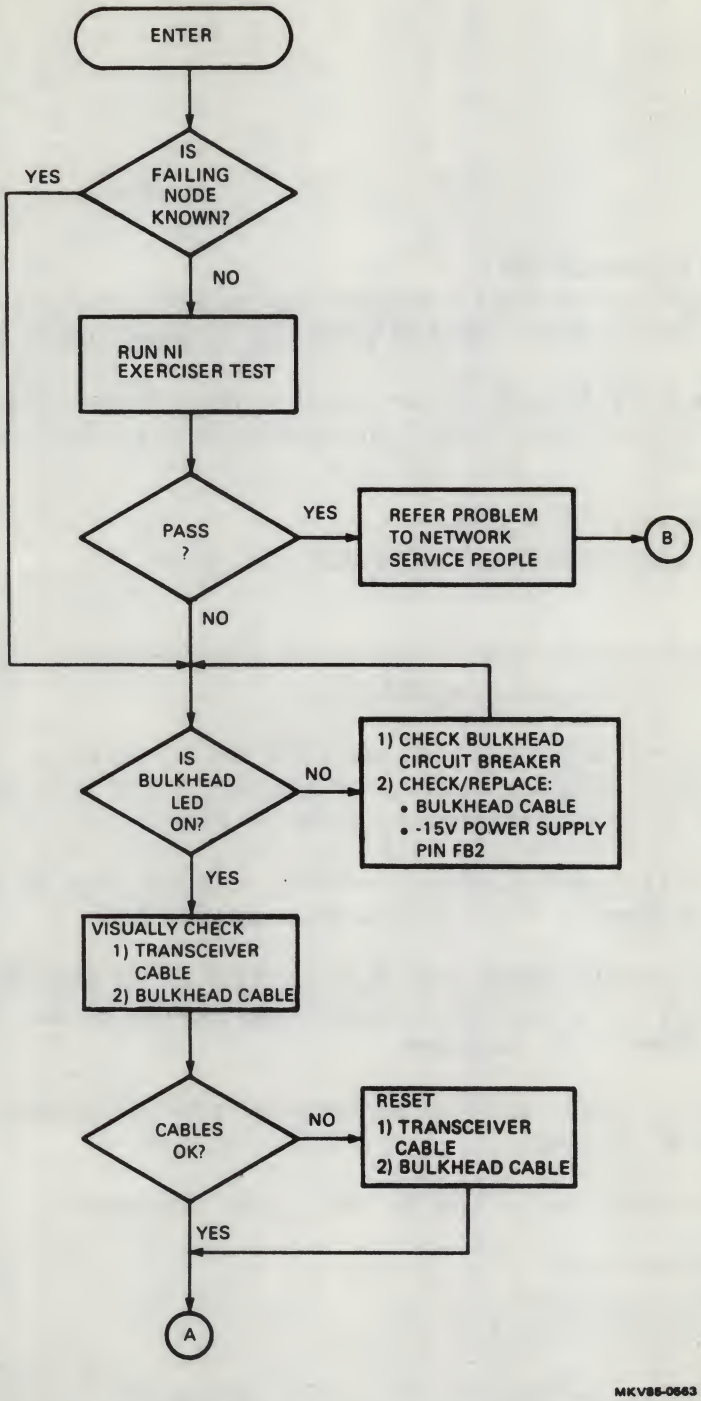


Figure 6-1 Troubleshooting Flowchart (Sheet 1 of 2)

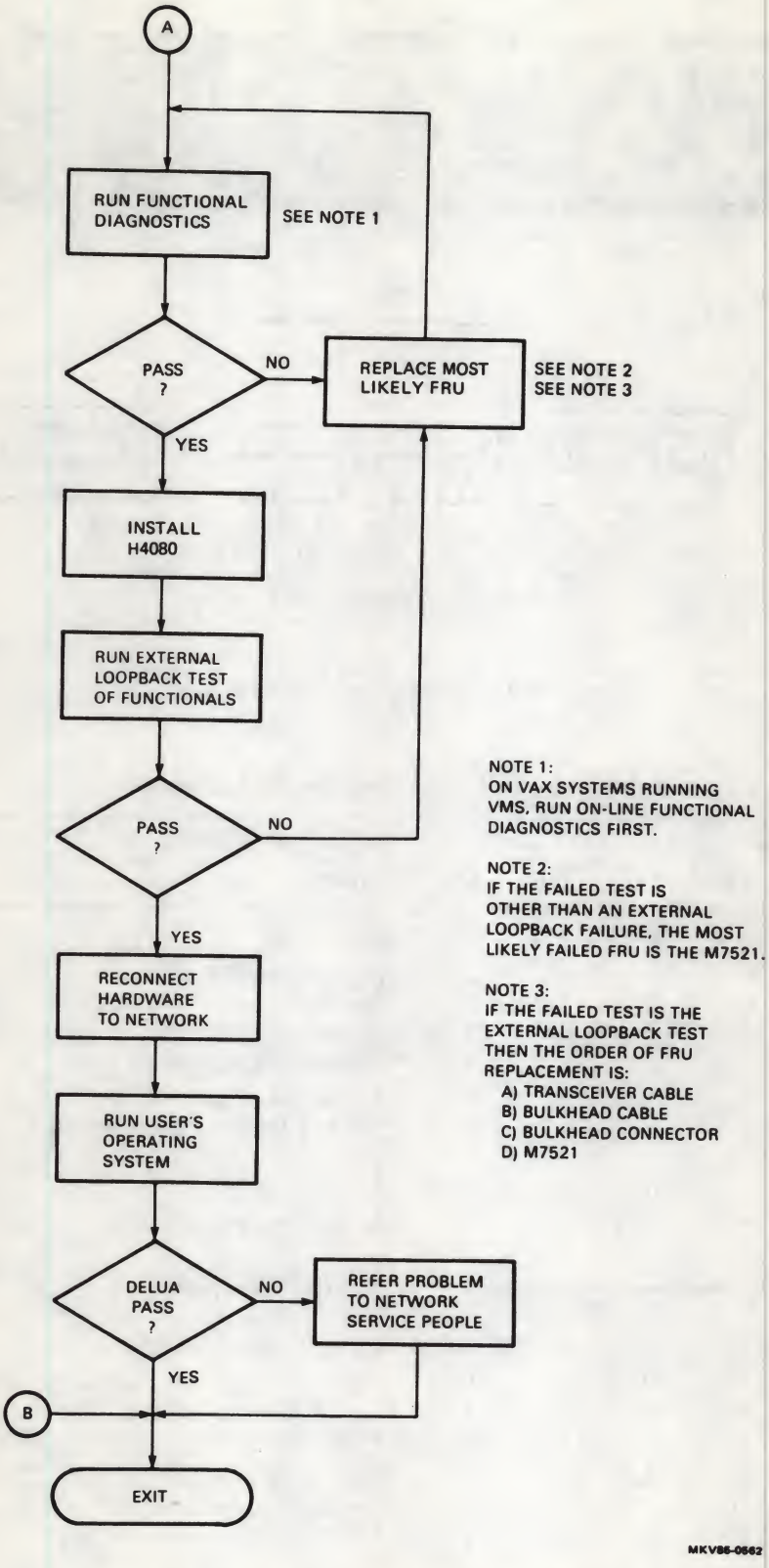


Figure 6-1 Troubleshooting Flowchart (Sheet 2 of 2)

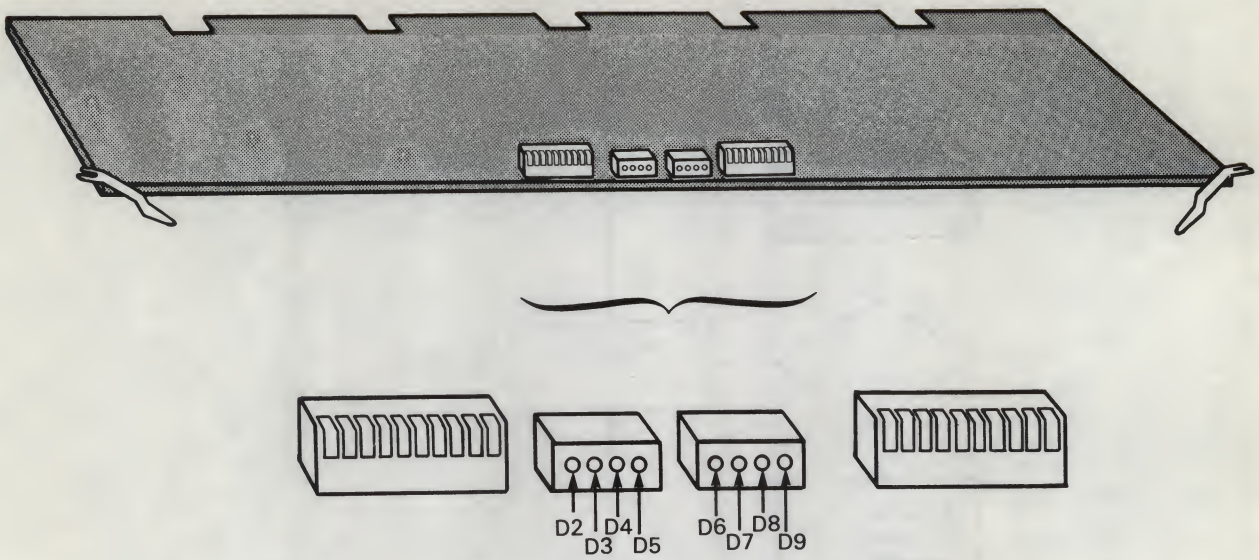


Figure 6-2 Selftest and Status LEDs

Table 6-1 Selftest Error and Status Codes

LEDs (1=ON)							
D3	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**Meaning**
0	0	X	0	0	0	0	Reset state
0	0	X	0	0	0	1	Primary load state
0	0	X	0	0	1	0	Ready state
0	0	X	0	0	1	1	Running state
0	0	X	0	1	0	1	UNIBUS halted state
0	0	X	0	1	1	0	NI halted state
0	0	X	0	1	1	1	NI and UNIBUS halted state
0	0	X	1	0	0	0	Port halted state
0	0	X	1	1	1	1	Secondary load state
		↑					**Activity Indicator**
0	1	0	0	0	0	1	Unsolicited trap
0	1	0	0	0	1	0	LANCE interrupt but no bits set in CSR0
0	1	0	0	0	1	1	LANCE memory error
0	1	0	0	1	0	0	Parity error
0	1	0	0	1	0	1	Port command 0 interrupt
0	1	0	0	1	1	0	Transmit error
0	1	0	0	1	1	1	MOP error
0	1	0	1	0	0	0	Receive error, dequeue from empty queue
0	1	0	1	0	0	1	Receive error, bad buffer being returned
0	1	0	1	0	1	0	Receive error, bad buffer being queued

Table 6-1 Selftest Error and Status Codes (Cont)

LEDs (1=ON)							
D3	D4	D5	D6	D7	D8	D9	Meaning
1	0	0	0	0	0	1	ROM CRC test
1	0	0	0	0	1	0	RAM checkerboard test
1	0	0	0	1	0	0	Nair, Thatte, and Abraham's memory test
1	0	0	0	1	0	1	RAM parity memory test
1	0	0	0	1	1	0	CPU microprocessor exception test
1	0	0	0	1	1	1	RAM parity interrupt test
1	0	0	1	0	0	0	Physical address ROM test
1	0	0	1	0	0	1	Timer interrupt test
1	0	1	0	0	0	0	LANCE internal loopback test
1	0	1	0	0	0	1	LANCE IBUS parity error test
1	0	1	0	0	1	0	LANCE CRC logic test
1	0	1	0	0	1	1	LANCE collision detection test
1	0	1	0	1	0	0	LANCE multicast address test
1	0	1	0	1	0	1	LANCE broadcast address test
1	0	1	0	1	1	0	LANCE physical address reject test
1	0	1	0	1	1	1	LANCE external loopback test
1	1	0	0	0	0	0	DMA block mover IBUS address register bit test
1	1	0	0	0	0	1	DMA block mover HBUS address register bit test
1	1	0	0	0	1	0	DMA block mover word count register bit test
1	1	0	0	0	1	1	DMA word mover HBUS address register bit test
1	1	0	0	1	0	0	DMA block mover ITEST test
1	1	0	0	1	1	0	DMA UNIBUS access test DMA failure
1	1	0	0	1	1	1	DMA UNIBUS access test UNIBUS NXM error
1	1	0	1	0	0	0	DMA word mover data register bit test
1	1	0	1	0	0	1	DMA word mover PCSR0 test
1	1	0	1	0	1	0	DMA word mover PCSR1, 2, 3 test
1	1	0	1	0	1	1	DMA block mover HBUS to IBUS test
1	1	0	1	1	0	0	DMA block mover IBUS to HBUS test
1	1	0	1	1	0	1	Port command interlock
1	1	1	0	0	0	0	DELUA IBUS loading test

6.2.2 DELUA VAX On-Line Functional Diagnostic (EVDYB*)

The DELUA VAX on-line functional diagnostic, EVDYB*, verifies all the DELUA functions that the VMS port driver program is capable of using. It is a VAX/VMS Level 2R (on-line only) diagnostic that runs under the VAX diagnostic supervisor (VDS).

Table 6-2 describes the tests performed by this diagnostic.

Table 6-2 DELUA VAX On-Line Functional Diagnostic (EVDYB*) Test Summary

No.	Name	Test
1	Read Internal ROM	The internal 16K byte ROM can be read and there are no CRC errors.
2	Read/Write Internal RAM	Data patterns can be written to and read from internal RAM memory.
3	Transmit CRC	The transmit CRC logic functions properly.
4	Receive CRC	The receive CRC logic functions properly.
5	Promiscuous Address	The DELUA in the promiscuous mode accepts all frames regardless of the destination address.
6	Enable All Multicast	The DELUA in the enable all multicast mode accepts all frames with multicast destination addresses.
7	Station Address	The DELUA recognizes the physical, multicast, and broadcast addresses of the node and discards frames with other addresses.
8	No Receive Buffers Available	The appropriate error will be flagged if a loopback is attempted and there are no receive buffers in host memory currently available (owned) by the DELUA.
9	DELUA Stress	The DELUA functions properly during heavy-traffic loading conditions.

6.2.3 DELUA PDP-11 Functional Diagnostic (CZUAD*)

The DELUA PDP-11 functional diagnostic, CZUAD, verifies all of the DELUA functions that the port driver program is capable of using. This diagnostic runs under the PDP-11 Diagnostic Supervisor and runs only in stand-alone mode.

The DELUA must be connected to an H4080 loopback transceiver to run this diagnostic. The diagnostic program assumes that the only frames to and from the transceiver are the frames that it has sent. If the DELUA is connected to a network and the diagnostic receives a frame sent by another node on the network, it reports errors.

Table 6-3 describes the tests performed by the DELUA PDP-11 functional diagnostic CZUAD*.

Table 6-3 DELUA PDP-11 Functional Diagnostic (CZUAD*) Test Summary

No.	Name	Test
1	PCSR0 READ ACCESS	A device is present at the PCSR0 UNIBUS address specified.
2	PCSR1 READ ACCESS	A device is present at the PCSR1 UNIBUS address specified.
3	PCSR1 DELUA ID BIT	Bit ⟨04⟩, and no other bits in the PCSR1 device ID field are set.
4	PCSR2 READ ACCESS	A device is present at the PCSR2 UNIBUS address specified.
5	PCSR3 READ ACCESS	A device is present at the PCSR3 UNIBUS address specified.
6	PCSR2 STATIC BIT	The test reads and writes each bit in PCSR2.
7	PCSR3 STATIC BIT	The test reads and writes each bit in PCSR2.
8	SELF TEST	Signals the DELUA to run its ROM-based diagnostic selftest.
9	PORT COMMAND	No errors occur when a DELUA port command is issued.
10	INTERRUPT LOGIC	The DELUA can generate an interrupt.
11	READ INTERNAL ROM	Internal ROM.
12	READ/WRITE INTERNAL MEMORY	Internal RAM can be written and read.
13	INTERNAL LOOPBACK	No errors occur when a frame is transmitted and received in internal loopback mode.
14	CRC CHECKING	CRC checking logic is operational.
15	FORCE CRC ERROR	CRC error detection is operational.
16	NO RECEIVE BUFFER	The appropriate error is flagged if a loopback is attempted and there are no receive buffers in host memory currently available (owned) by the DELUA.
17	DISABLE RECEIVE	The appropriate error is flagged if CHAINING the receive buffer in host memory is too small and receive chaining is disabled so that the DELUA cannot place the rest of the frame in another receive buffer.
18	TRANSMIT CHAINING ERROR	The DELUA can set the buffer length error (BUFL) in the transmit descriptor ring.

Table 6-3 DELUA PDP-11 Functional Diagnostic (CZUAD*) Test Summary (Cont)

No.	Name	Test
19	DATA CHAINING	The DELUA can chain together more than one transmit data buffer and send the data as a single frame. Also, when the DELUA receives a frame that is larger than the receive data buffer, it continues the frame into the next receive data buffer.
20	PHYSICAL ADDRESS	When the DELUA is set to ignore multicast frames, it receives only frames sent to its Ethernet physical address.
21	MULTICAST ADDRESS	When the DELUA is set to receive multicast frames, it receives frames of the specified multicast groups.
22	PROMISCUOUS ADDRESS	When the DELUA is set to receive frames from all Ethernet addresses, it does.
23	ENABLE ALL MULTICAST	The DELUA in multicast mode accepts all frames with multicast destination addresses.
24	INTERNAL LOOPBACK TRANSMIT LENGTH ERROR	The DELUA flags an error when the diagnostic attempts to send an internal loopback frame that is longer than 36 bytes or 32 bytes if DTCR is 0. See Section 5.1.
25	SIMULTANEOUS OPERATIONS	Simultaneous operations can be performed.
26	EXTERNAL LOOPBACK (Manual Intervention Required)	Using an external loopback connector, this ensures that no errors occur when a frame is transmitted and received in external loopback mode.
27	PRINT DEVICE	Prints the default physical address, PARAMETERS the microcode revision, and the switch pack settings.

6.2.4 DEC/X11 DELUA Test CXUAD*

The DEC/X11 DELUA test achieves maximum UNIBUS activity by transmitting many frames of data.

The DELUA must be connected to an H4080 loopback transceiver to run this diagnostic. The diagnostic program assumes that only the frames to and from the transceiver are the frames that it has sent. If the DELUA is connected to a network and the diagnostic receives a frame sent by another node on the network, it reports errors.

6.2.5 NI Exerciser CZUAC*/EVDWC*

The Network Interconnect Exerciser (NIE) sets up frame traffic between many nodes on the network. Refer to the *Network Interconnect Exerciser User's Guide* (order number AA-HI06A-TE) for information on the NI Exerciser diagnostic test.

APPENDIX A
FLOATING DEVICE ADDRESSES AND VECTORS

A.1 FLOATING DEVICE ADDRESSES AND VECTOR ADDRESSES

UNIBUS addresses from 760010 through 763776 are floating device addresses (see Figure A-1) used as register addresses for devices interfacing with a PDP-11 or VAX system.

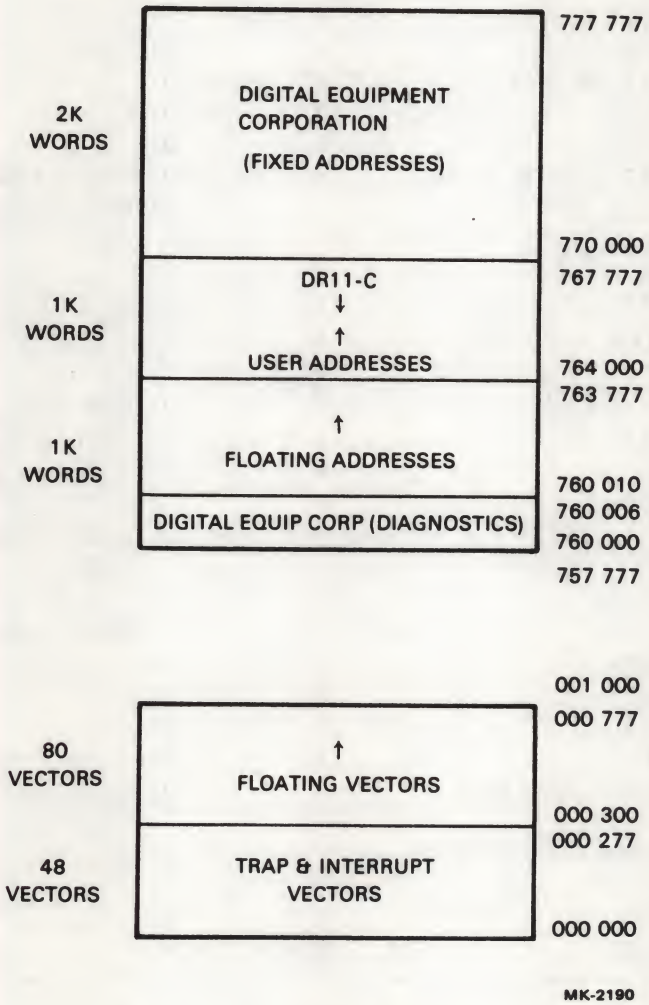


Figure A-1 UNIBUS Address Map

A.2 FLOATING DEVICE ADDRESSES

Assign device addresses according to the following procedure to allow the auto-configuration program to properly configure the operating system to communicate with all devices that use the floating addresses.

Assign addresses to devices according to the order in which they are shown in Table A-1. The floating address space starts at 760010. The DJ11 option is the first device in the table. If the system has a DJ11 option, assign it address 760010. If the system has another DJ11 option, add the octal modulus shown in Table A-1 to determine the address (760020 in this case). Leave a gap of octal 10 unused addresses when switching to a new device type. Leave a gap of octal 10 unused addresses for each type of device that does not exist in the system. The example in Section A.4 shows how this address assignment procedure is used.

Table A-1 Floating Device Address Ranking Sequence

Priority Rank	Option	Decimal Size	Octal Modulus
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11, DUV11	4	10
5	DUP11	4	10
6	LK11-A	4	10
7	DMC11/DMR11	4	10 (DMC11 before DMR11)
8	DZ11*/DZV11, DZS11/DZ32	4	10 (DZ11 before DZ32)
9	KMC11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11,RLV11	4	10 (after first)
15	LPA11-K	8	20 (after first)
16	KW11-C	4	10
17	Reserved	4	10
18	RX11/RX211 RXV11/RXV21	4	10 (after first) (RX11 before RX211)
19	DR11-W	4	10
20	DR11-B	4	10 (after second)
21	DMP11	4	10
22	DPV11	4	10
23	ISB11	4	10
24	DMV11	8	20
25	DEUNA/DELUA	4	10 (after first) (DEUNA before DELUA)
26	UDA50	2	4 (after first)
27	DMF32	16	40
28	DMS11	6	20
29	VS100	8	20

* DZ11-E and DZ11-F are considered as two DZ11 options.

A.3 FLOATING VECTOR ADDRESSES

UNIBUS addresses from 300 to 777 are floating vector addresses used for devices interfacing with a PDP-11 or VAX system.

Do not leave any gaps of unused addresses between floating vector addresses unless they are required by the physical hardware of the device. In data communications devices, the receive vector must be on a zero boundary; the transmit vector must be on an octal 4 boundary.

Multiple devices of the same type should be assigned vectors sequentially. Table A-2 lists the floating vector assignment sequence.

Table A-2 Floating Vector Assignment Sequence

Priority Rank	Option	Decimal Size	Octal Modulus
1	DC11*	4	10
1	TU58*	4	10
2	KL11†	4	10
2	DL11-A†	4	10
2	DL11-B†	4	10
2	DLV11-J†	16	10
2	DMV11, DLV11-F†	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB/BA	2	4
7	DH11 modem control	2	4
8	DR11-A, DRV11-B	4	10
9	DR11-C, DRV11	4	10
10	PA611 (reader+punch)	8	10
11	LPD11	4	10
12	DT07	4	10
13	DX11	4	10
14	DL11-C	4	10
14	DL11-D	4	10
14	DL11-E/DLV11-E	4	10
15	DJ11	4	10
16	DH11	4	10
17	GT40	8	10
17	VSV11	8	10
18	LPS11	12	10
19	DQ11	4	10
20	KW11-W, KWV11	4	10
21	DU11, DUV11	4	10
22	DUP11	4	10
23	DV11+modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10 (DMC before DMR)
27	DZ11/DZV11,	4	10 (DZ11 before DZ32)

Table A-2 Floating Vector Assignment Sequence (Cont)

Priority Rank	Option	Decimal Size	Octal Modulus
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11	2	4 (after the first)
35	TS11	2	4 (after the first)
36	LPA11-K	4	10
37	IP11/IP300	2	4 (after the first)
38	KW11-C	4	10
39	RX11/RX211 RXV11/RXV21	2	4 (after the first) (RX11 before RX211)
40	DR11-W	2	4
41	DR11-B	2	4 (after the first)
42	DMP11	4	10
43	DPV11	4	10
44	ML11	2	4 (MASSBUS device)
45	ISB11	4	10
46	DMV11	4	10
47	DEUNA/DELUA	2	4 (after the first) (DEUNA before DELUA)
48	UDA50	2	4 (after the first)
50	KMS11	6	10
51	PCL11-B	4	10
52	VS100	2	4

* There is no standard configuration for systems that contain both a DC11 option and a TU58 option.

† A KL11 option or DL11 option used as the console, uses a fixed vector.

A.4 DEVICE AND VECTOR ADDRESS ASSIGNMENT EXAMPLE

This section contains an example of how to assign floating device and vector addresses. This system contains the following devices to be assigned floating addresses.

1 DJ11	2 DUP11s
1 DH11	2 DMR11s
2 DQ11s	2 DELUAs

The devices for this system should be assigned device and vector addresses as shown in Table A-3.

Table A-3 Device and Vector Address Assignments

Option	Device Address	Vector Address	Comment
DJ11	760010	300	Only one DJ11 option
	760020		Gap left between DJ11 option and the next device
	760030		Gap – The next device, a DH11 option, must start on an address boundary that is a multiple of 20
DH11	760040	310	Only one DH11 option
	760060		Gap left between DH11 option and the next device
DQ11	760070	320	First DQ11 option
DQ11	760100	330	Second DQ11 option
	760110		Gap between last DQ11 option used and the next device
	760120		Gap left for DU11 option (none in system)
DUP11	760130	340	First DUP11 option
DUP11	760140	350	Second DUP11 option
	760150		Gap left between last DUP11 option and the next device
	760160		Gap left for LK11-A option (none in system)
DMR11	760170	360	First DMR11 option
DMR11	760200	370	Second DMR11 option
	760210		Gap left between last DMR11 option and the next device
	760220		Gap left for DZ11 option (none in system)
	760230		Gap left for KMC11 option (none in system)
	760240		Gap left for VMV21 option (none in system)
	760260		Gap left for VMV31 option (none in system), must start on an address boundary that is a multiple of 20 and also leave a gap of 20
	760300		Gap left for DWR70 option (none in system)
	760310		Gap left for RL11 option (none in system)

Table A-3 Device and Vector Address Assignments (Cont)

Option	Device Address	Vector Address	Comment
	760320		Gap left for LPA11-K option (none in system), must start on an address boundary that is a multiple of 20 and also leave a gap of 20
	760340		Gap left for KW11-C option (none in system)
	760350		Gap left for reserved device
	760360		Gap left for RX11 option (none in system)
	760370		Gap left for DR11-W option (none in system)
	760400		Gap left for DR11-B option (none in system)
	760410		Gap left for DMP11 option (none in system)
	760420		Gap left for DPV11 option (none in system)
	760430		Gap left for ISB11 option (none in system)
	760440		Gap left for DMV11 option (none in system), must start on an address boundary that is a multiple of 20 and also leave a gap of 20
DEUNA or DELUA	774510	120	First DEUNA/DELUA uses fixed device and vector addresses
DEUNA or DELUA	760460	400	Second DEUNA/DELUA uses floating device and vector addresses

INDEX

Zu AABd = Derma repair Diagn.

Zu ACCd = Derma (chI) Exercises.

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